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Design and Comparison of Full Adder Using TG Based 4:1 MUX

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ABSTRACT

The various analyses are based primarily on arithmetic circuit, notably with MUX design , however this paper also investigates using a multiplexer to reduce power consumption. A 4:1 MUX is designed using CMOS transmission gate logic (TGL), which has lower circuit complexity than traditional CMOS-based multiplexers. The NMOS and PMOS are coupled for a strong output level with a gain in area, which is the central outcome of the proposed MUX. The designed circuit is dissipating 27.93 µW from a 1.8 V supply voltage in comparison to 43.85 µW of conventional full adder.

Keywords: Mux, Full Adder, Transmission Gate, CMOS.

INTRODUCTION

One of the most crucial considerations in system SOC design is low power consumption, and technologies for low-power designs in applications requiring high speed interfaces are being created and put to the test in actual design projects. Multiplexers are crucial components of CMOS memory and data processing systems. Various design stages, including architectural, circuit, layout, and process technologies, can be attributed for the rising demand for low power VLSI. The multiplexer, often known as MUX, is the brain of any arithmetic circuit. MUX is used as a standard building component for data paths and data-switching architectures in processors, processor buses, network switches, and DSPs with resource sharing. There are two different Digital Logic circuits: multiplexer and full adder. Multiplexer is also a digital switch. It enables the routing of digital data from several sources into a single output line. Comparatively, the Full adder circuit adds three bits and generates the sum and carry as its output. Instead of employing the standard basic logic gates, this study suggests using multiplexers in a full adder circuit.

MATERIALS & METHODS

A. Full Adder Using 4:1 TGL Based Mux

The creation of the full adder's truth table is necessary before implementing a full adder using MUX. Table 1 displays the truth table for the full adder.

TABLE I: TRUTH TABLE OF A FULL ADDER

A	B	Cin	SUM	Cout
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

The minterms for the Sum and Carry outputs from the truth table are determined.

For Sum- $f(A, B, Cin) = \sum (1,2,4,7)$ (1)

For Carry- $f(A, B, Cin) = \sum (3,5,6,7)$ (2)

As per the design table 1, input to the first Mux is of Sum, A0 = A, A1 = A', A2 = A', A3 =A. The input to the second Mux is of Carry, A0 = 0, A1 = A, A2 = A,A3 = 1. The B & Cin input is connected to the selection line of the first and second Mux. The proposed full adder is as shown in Fig.1.

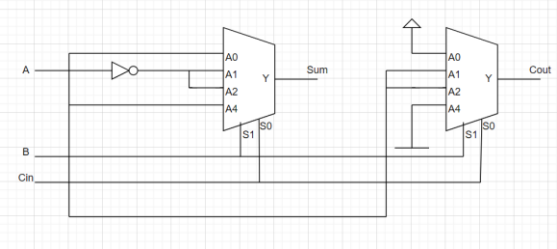

Fig.1. FULL ADDER USING MUX

The Sum will be presented as the output of the first MUX, and the Cout will be displayed as the output of the second MUX. There are multiple applications where a full adder is employed, some of which include the fundamental building blocks of an on-chip libraries and in processors and other kinds of computing devices like the arithmetic logic unit (ALU). In this project, a full adder is built using a MUX that was first built using TGL, and the performance results are compared to those of a traditional full adder. Figure 1 illustrates the 4:1 Mux construction using TGL. There are four lines. The following four signals—X0, X1, X2 and X3—must be multiplexed on a single line: output. The Data Inputs are another name for the four input lines. Since there are four inputs, the multiplexer needs two more inputs, known as the Select Inputs , to determine which of the X inputs will appear at the output. These select inputs are designated as select lines C0 and C1. The transmission gate can be used to quickly isolate many signals with little board space investment and with little deterioration of those vital signals' essential properties. The solid state-switch is comprised of parallel connection of a PMOS transistor and NMOS transistor. Both transistors are either on or off owing to complementary biassing of the control gates. The proposed structure uses the least amount of area while reducing power consumption. Multiplexers can be used to construct any logic function, from simple gates to complicated functions. The full adder circuit, whose truth table is illustrated in Table I, is built in Cadence Virtuoso using a 4:1 multiplexer as shown in Fig.2. To implement a full adder two 4:1 MUX is required where one of the MUX outputs will give the expression for Sum and the other one for Carry Out. Representing logical operation with MUX is a clever manipulation. Hence, the selection lines and the inputs are set up so that the Sum can be easily represented using the remaining input manipulation.

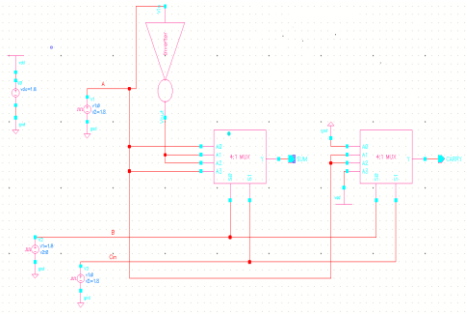

Fig.2. 4:1 PROPOSED FULL ADDER DESIGN USING TG 4:1 MUX

Consider S0 and S1 as the selection lines; now observe the correlation between the remaining input Cin and Sum. For S0S1 = 00, Sum = Cin. This is the case for S0S1=11 as well and for the remaining cases Sum = ~Cin. Therefore inputs for the MUX are going to be as shown in Table II.

TABLE II: CONFIGURING THE INPUTS

Input Lines	Input Configured
A0	Cin
A1	~Cin
A2	~Cin
A3	Cin

Elaborating further the internal circuitry of the proposed 4:1 MUX using TG is shown below in Fig.3. With little investment in board space and negligible loss of those critical signals' properties, the transmission gate can be utilised to swiftly isolate a number of signals. An electronic component

called a "transmission gate" is described as one that will selectively block or allow a signal level to pass from the input to the output. The complementary Logic 1 is applied to node active-low S0 when the voltage on node S0 is a Logic 0, allowing both transistors to conduct and pass the signal at node A0 to Y. The complementary Logic 1 is applied to node active low S0 when the voltage there is a Logic 0, turning off both transistors and causing a high impedance situation on both the A0 and Y nodes. The schematic diagram in Fig. 3 contains the arbitrary labels for A0 and Y because switching those labels around won't change how the circuit functions. With no loss of input signal quality, this architecture offers full bidirectional connection.

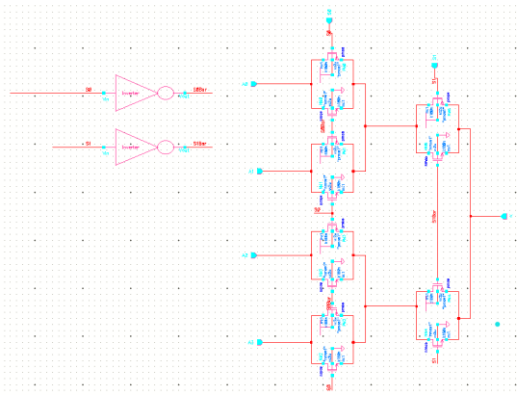

Fig.3. 4:1 MUX USING TRANSMISSION GATE LOGIC

B. Conventional Full Adder Using Basic Gates

A conventional full adder using different basic and arithmetic gates is shown in Fig.4. Here 2 AND, 2 XOR and 1 OR gate is used to implement a full adder circuit based on the Truth table as in Table 1. The working principle remains the same except the way how this circuit is constructed. In Cadence Virtuoso these gates are again constructed using PMOS and NMOS transistors leading to different issues in area, power, and propagation delay.

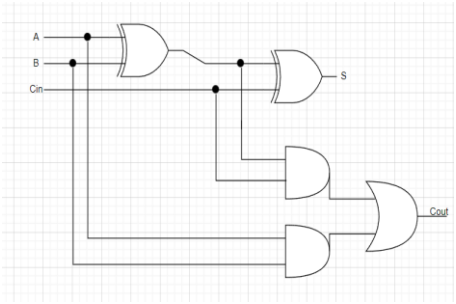

Fig.4. CONVENTIONAL FULL ADDER

In a bit to compare and analyze the difference between a conventional adder and an adder using MUX, a conventional adder built using basic CMOS logic is as shown above in Fig. 5. The working principle remains the same, a detailed comparison between the two is discussed below using the output waveforms and the difference in area, power and propagation delay each offered during the process.

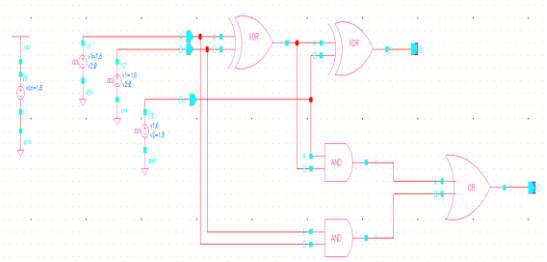

Fig.5. CONVENTIONAL FULL ADDER SCHEMATIC

RESULT

A. Output waveforms and power calculations

The output waveform of proposed full adder using TGL is shown in Fig.6. and the corresponding waveform achieved for the conventional full adder schematic is shown in Fig.7.

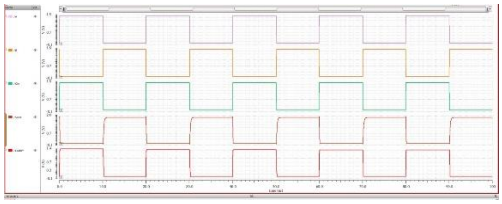

Fig.6. OUTPUT OF PROPOSED ADDER

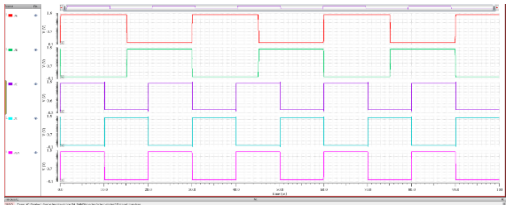

Fig.7. OUTPUT OF CONVENTIONAL ADDER

Average power consumed by both conventional and proposed full adder was obtained from the virtuoso tool. It is observed that the proposed adder has a power dissipation of 27.93µW compared to 43.85µW which is observed in the conventional circuit. There is also a considerable decrease in area as the transistor count is reduced from 50 to 34 in the proposed circuit. The maximum propagation delay of proposed full adder is 141ps in comparison with 183ps of conventional full adder.

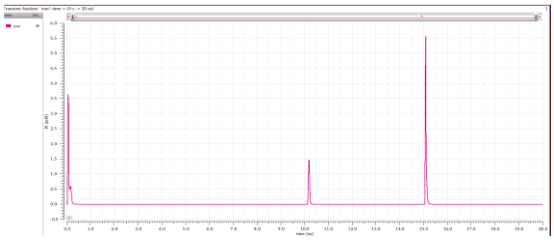

Fig.8. AVERAGE POWER GRAPH OF PROPOSED ADDER

B. Result Analysis

TABLE III: PERFORMANCE ANALYSIS

Design	Power Dissipation	Propagation Delay	Transistor Count
Conventional Full Adder	43.85µW	141ps	50
Proposed Full Adder	27.93µW	183ps	34

Fig.9. GRAPH COMPARING POWER AND AREA OF PROPOSED AND CONVENTIONAL ADDER

CONCLUSION

A Full adder implementation using TGL based MUX is proposed in the paper. The full adder's performance is evaluated in terms of power consumption, propagation latency, and transistor count. The proposed design is contrasted with a standard Full Adder constructed using CMOS. After examining the findings, it is clear that the suggested adder outperforms the conventional adder in terms of transistor count and power consumption. The power dissipation reduces to 27.93µW compared to 43.85µW of conventional adder and transistor count has reduced to 34 in proposed adder compared to 50 in conventional adder.

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Conflict of Interest: None

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