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Leakage Power Reduction in CMOS Logic Circuit Using Various Techniques

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ABSTRACT

Low power nowadays High-power consumption has turned into a crucial design criterion for VLSI an emerging field. When it comes to energy efficiency, high power dissipation is not thought to be beneficial to battery life in the case of battery-powered applications. It reduces the efficiency, dependability, and cooling expenses of battery life. The high-frequency dynamic variation of inputs is heavily influenced by switching and short-circuit leakage power. There are several common methods for reducing the power consumption of circuits. The average power consumption consists of static and dynamic power consumption. The power consumption comparison of LECT0R, LCNT, Stack 0N0FIC, and SAP0N of various low-power techniques. These circuits are simulated in the cadence tool.

Keywords: LECT0R, LCNT, Stack 0N0FIC, and SAP0N Techniques, cadence tool (90nm).

INTRODUCTION

Digital portable systems are under more and more pressure to be energy efficient in today's technologies. In VLS1 technology [9], size, power consumption, and Significant design characteristics include propagation delay. But the use of low-power design has grown in importance in device portability in order for VLSI systems to perform well, A serious issue is excessive power use a lot of power Consumption decreases battery life and needs more cooling and packing fees. Many factors affect how much power is used, consisting of operating frequency, transistor count, and the most advancing technology that has an impact. power in excess Consumption causes devices to heat up, reducing their dependability, efficiency, and performance. Simulation of these was done in the cadence tool and tabulated the power consumption by using these techniques.

I. POWER CONSUMPTION

The power consumption of the circuit is the sum of Static power and Dynamic power.

A. Dynamic power:

The parasitic capacitor charges and discharges when a toggle is made from 0 to 1 or vice versa. Dynamic consumption results from this charging and discharging. The formula for dynamic power consumption is provided by.

$$P = \alpha * f * C * V_{dd}^2 \quad (1)$$

where,
α - switching activity
f - frequency
C – load capacitance
V_{dd} - supply voltage

B. Static power leakage:

The sub-threshold channel conductance current and reverse bias P-N junction current are the main causes of leakage power. When the leakage current falls below the threshold voltages, sub-threshold power results. The following elements influence subthreshold leaking,

• Thermal voltage (Vth),

• Difference between the actual gate voltage (Vg) and threshold voltage (Vt).

The reverse-biased PN junction current is given by

$$I_D = Is\ (e^{V/Vt}-1) \qquad (2)$$

C. Short Circuit Leakage Power:

Dynamic power consumption is significantly impacted by short circuit leakage [12]. There is a period during the transition when the gates' voltage is between the NM0S and PM0S thresholds, turning on both transistors [1]. Due to the nature of the CM0S architecture [9], power loss results from the formation of a straight conducting line from the voltage source to the ground while both transistors are in the 0N state. This power is influenced by the length, incline, and 1-V curve of the transistor loading capacitances.

$$P = I_{mean} * V \qquad (3)$$

DESIGN METHODOLOGY

A. Inverter:

In the conventional CM0S logic inverter, the source terminals of the PM0S transistor and NM0S transistors are connected to Vdd and ground, respectively. The drain terminals are where the output is obtained, and the input is connected to the gate terminals. as shown in Fig. 1.1. If the input is logical high its output will be logic zero and vice versa

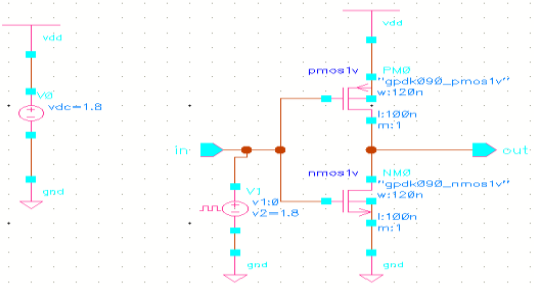

Fig.1.1 Inverter

B. LECTOR:

In this method, leakage-controlled transistor PM0S and NM0S transistors are inserted between logic cells, as shown in Fig. 2.1, with each transistor's gate terminal coupled to the source of another transistor [3]. Low power consumption is the result of the efficient stacking of transistors between the supply voltage (V_{dd}) and GND (ground) [7]. One transistor in the logic circuit remains in the cut-off zone throughout each step of the input cycle, for current flow it provides resistance and lowers power consumption [13].

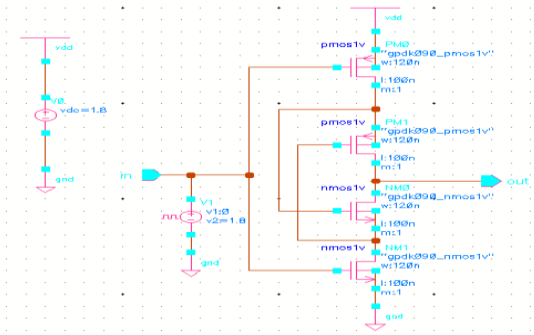

Fig.2.1 LECT0R Inverter

C. LCNT:

It is also one of the techniques for leakage reduction in which, as illustrated in Fig. 3.1, two leakage-controlled NM0S transistors are added between the logic cells with both of their gate terminals linked to the output node [4]. So, by making the path between the supply voltage (V_{dd}) and the GND (ground) more resistant, less power is used. This technique's utility in driven circuits is reduced by the drawback that it cannot pull up or pu1l down to the precise value.

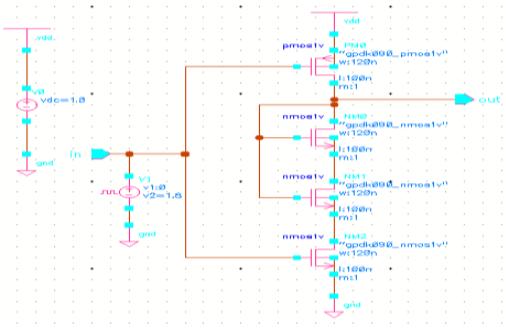

Fig.3.1 LCNT Inverter

D. Stack ONOFIC:

The inclusion of a PM0S transistor LCNT circuit is Stack ONOFIC (ON or OFF). The drain terminal of the PM0S transistor is to two NMOS transistors gate terminals [5], the NM0S is series with the logic. The gate

terminal of PMOS connected to the output as shown in Fig. 4.1. The block that was put into the logic is known as the Stack 0N0FIC block [3]. This block presents the lowest ON state hindrance and the highest OFF state hindrance. Low power reduction is achieved in this way.

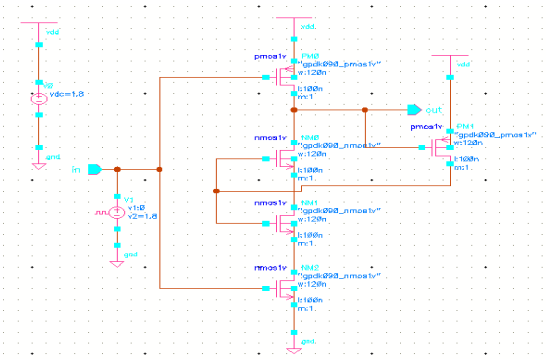

Fig.4.1 Stack 0N0FIC Inverter

E. SAPON:

In this technique the resistance between the supply voltage (V_{dd}) and GND (ground), is by connecting two leakage-control transistors outside the logic. This prevents leakage current from a short circuit during the changeover stage. In addition, it uses CM0S SAP0N transistors connected in series between the supply voltage (V_{dd}) and the GND (ground) to manage the sub-threshold leakage current during the leve1ing phase. NM0S and PM0S SAP0N Transistors' gate terminals are connected to ground (GND) and Vdd (supply voltage), respectively. According to Fig. 5.1, SAP0N PM0S is positioned above the pull-up network, while SAP0N NM0S is positioned below the pull-down network. Due to the need to function in an active region, these two SAP0N transistors are active during all phases. Consequently, it produces desired results while yet using little electricity.

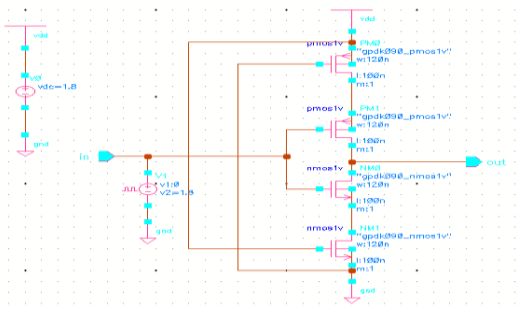

Fig.5.1 SAP0N 1nverter

F. NOR:

A NOR gate is a type of digital logic gate that gives logic high output if all the inputs are 0 and gives logic low output if any one of the inputs is 1. As long as the input voltage is less than the threshold, logic 0 is the output of the NOR. Fig.1.2 Shows the schematic of NOR.

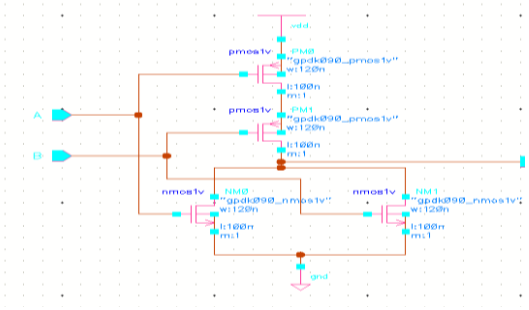

Fig.1.2 NOR

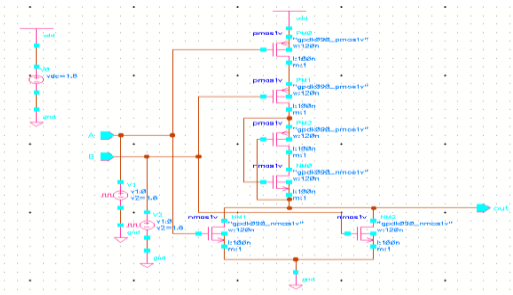

Fig.2.2 LECTOR NOR

In LECTOR NOR two leakage-controlled transistors of PMOS and NMOS transistors are connected between logic cells, as shown in Fig. 2.2.

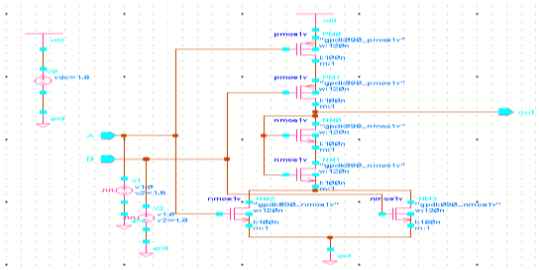

Fig.3.2 LCNT NOR

In the LCNT NOR in between the logic cell, two NM0S leakage-controlled transistors are added with both of their gate terminals linked to the 0utput node as shown in Fig.3.2.

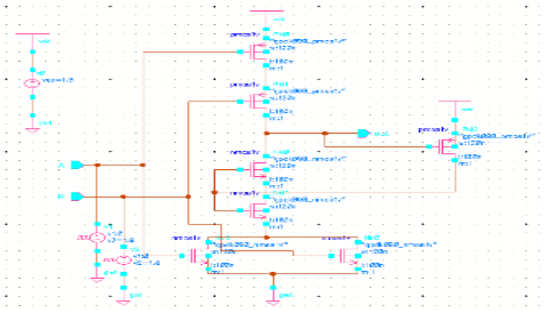

Fig.4.2 Stack 0NOFIC NOR

In the Stack, ONOFIC the PMOS transistor, and the drain terminal are connected to two series-connected NMOS transistors and the PMOS gate termina1 is connected to the 0utput node. as shown in Fig. 4.2.

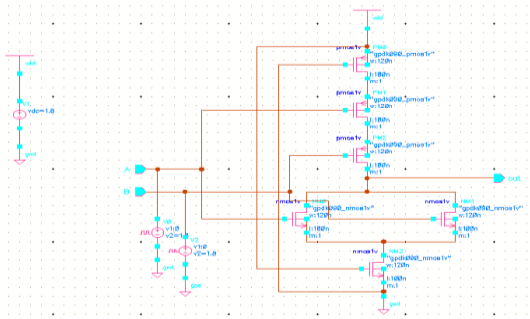

Fig.5.2 SAPON NOR

In the SAPON PMOS and NMOS SAPON Transistors' gate terminals are connected to the supply voltage (V_{dd}) and the GND (ground), respectively. According to Fig. 5.2, SAP0N PM0S is positioned above the pull-up network, while SAP0N NM0S is positioned below the pull-down network.

SR Flip Flop:

The flip-flop has two complementary outputs that are Q and Q and two inputs that are R and S. It's necessary to keep in mind that logic '1' is a dominating input for NOR gates, which means that if any one of its inputs is logic '1' (HIGH), the output will always be logic '0' (L0W), regardless of the other input. By using NOR of different techniques design the SR Flip Flop circuit.

TABLE 3. Truth Table of SR Flip Flop

R	S	Q	State
0	0	Last state	No change
0	1	1	Set
1	0	0	Reset
1	1	Not applied	Forbidden

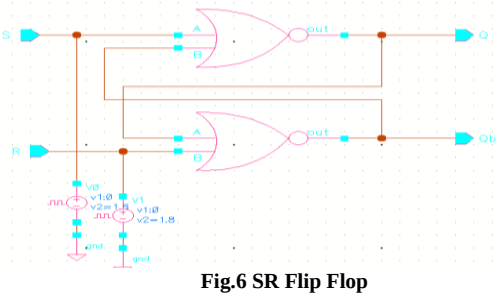

Fig.6 SR Flip Flop

SIMULATION AND RESULT

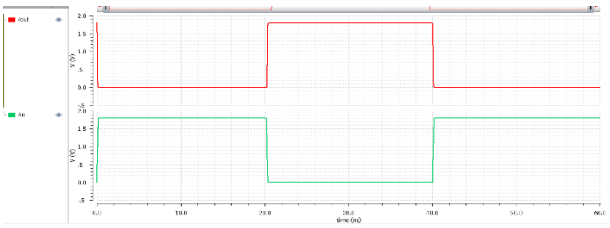

Fig.1.3 Transient analysis of INVERTER

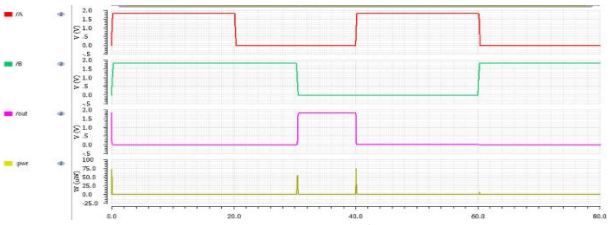

Fig.1.4 Transient analysis of NOR gate

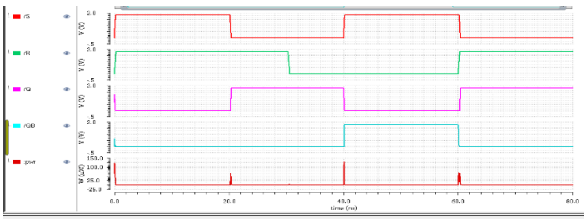

Fig.1.5 Transient analysis of SR Flip Flop

Fig.1.3, 1.4, 1.5 shows the Transient analysis of INVERTER, NOR, and SR Flip Flop respectively.

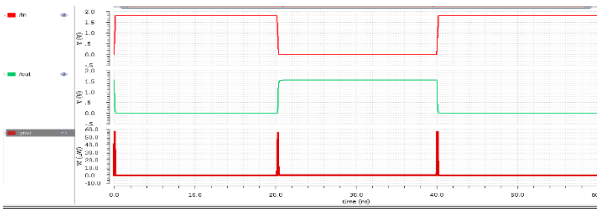

Fig.2.3 Transient analysis of LECTOR INVERTER

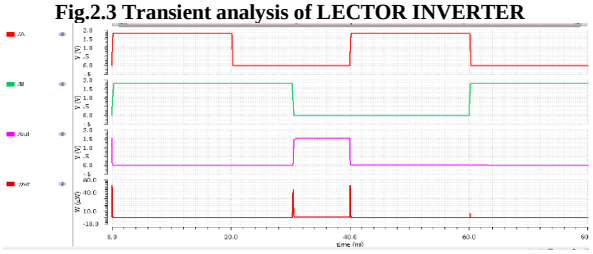

Fig.2.4 Transient analysis of LECTOR NOR

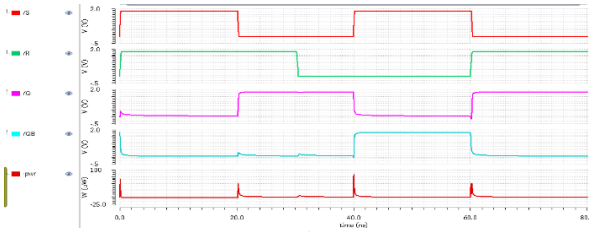

Fig.2.5 Transient analysis of LECTOR SR Flip Flop

Fig.2.3, 2.4, 2.5 shows the Transient analysis of LECTOR INVERTER, NOR, and SR Flip Flop respectively.

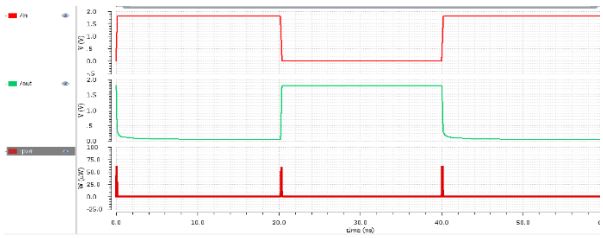

Fig.3.3 Transient analysis of LCNT INVERTER

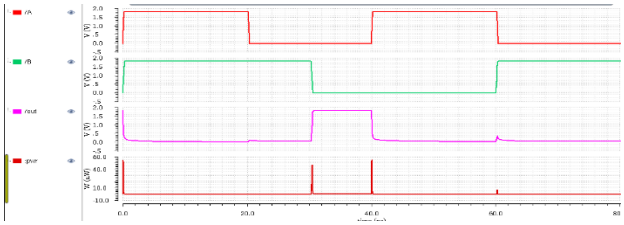

Fig.3.4 Transient analysis of LCNT NOR

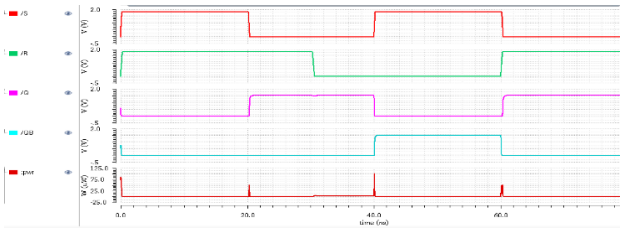

Fig.3.5 Transient analysis of LCNT SR Flip Flop

Fig.3.3, 3.4, 3.5 shows the Transient analysis of LCNT INVERTER, NOR, and SR Flip Flop respectively.

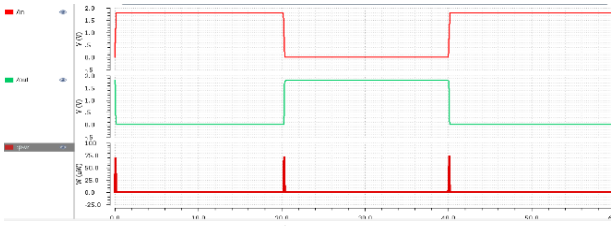

Fig.4.3 Transient analysis of Stack ONOFIC INVERTER

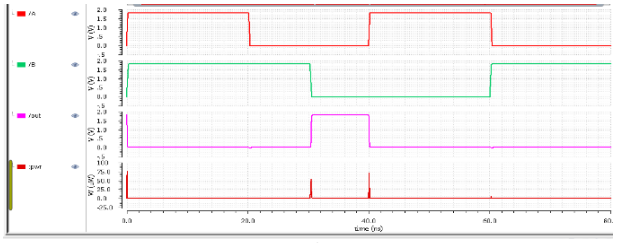

Fig.4.4 Transient analysis of Stack ONOFIC NOR

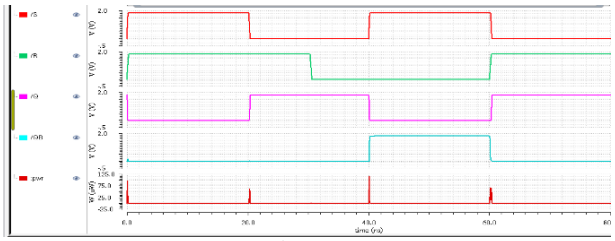

Fig.4.5 Transient analysis of Stack ONOFIC SR Flip Flop

Fig.4.3, 4.4, and 4.5 shows the Transient analysis of Stack ONOFIC INVERTER, NOR, and SR Flip Flop respectively.

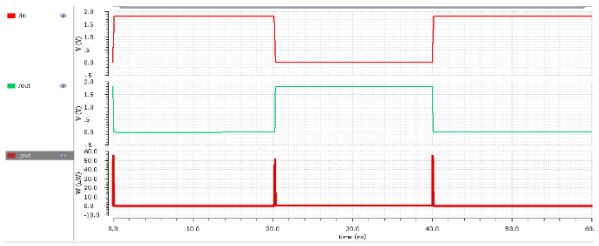

Fig.5.3 Transient analysis of SAPON INVERTER

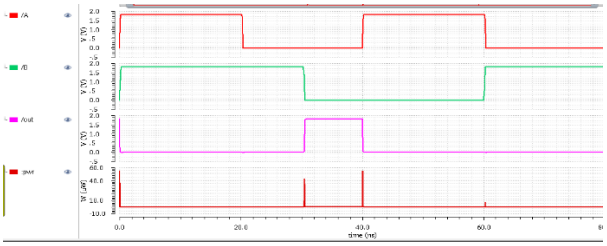

Fig.5.4 Transient analysis of SAPON NOR

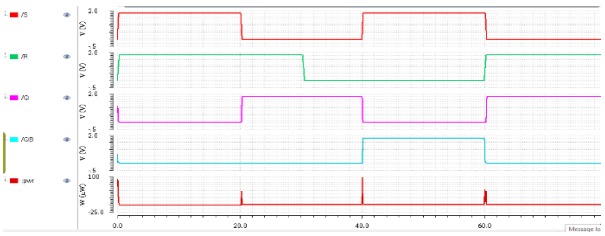

Fig.5.5 Transient analysis of SAPON SR Flip Flop

Fig.3.3, 3.4, 3.5 shows the Transient analysis of SAPON INVERTER, NOR, and SR Flip Flop respectively.

TABLE 4. Power Analysis of INVERTER

Techniques	Number of Transistor	Total Power = Static Power + Dynamic Power (μW)
Normal	2	77.69
LECTOR	4	57.19
LCNT	4	61.82
Stack ONOFIC	5	73.52
SAPON	4	55.34

TABLE 5. Power Analysis of NOR

Techniques	Number of Transistor	Total Power = Static Power + Dynamic Power (μW)
Normal	4	73.25
LECTOR	6	51.31
LCNT	6	55.02
Stack ONOFIC	7	75.52
SAPON	6	51.02

TABLE 6. Power Analysis of SR Flip Flop

Techniques	Number of Transistor	Total Power = Static Power + Dynamic Power (μW)
Normal	8	129.85
LECTOR	12	84.35
LCNT	12	101.65
Stack ONOFIC	14	115.58
SAPON	12	81.18

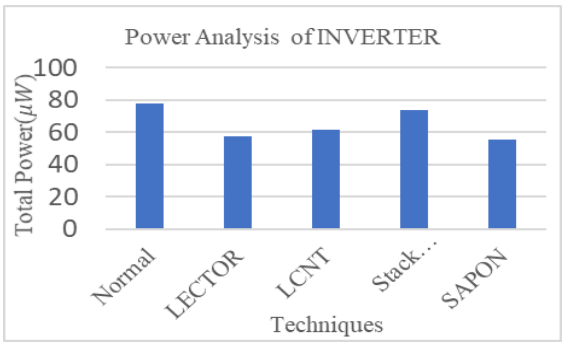

Fig.7 Power Analysis of INVERTER

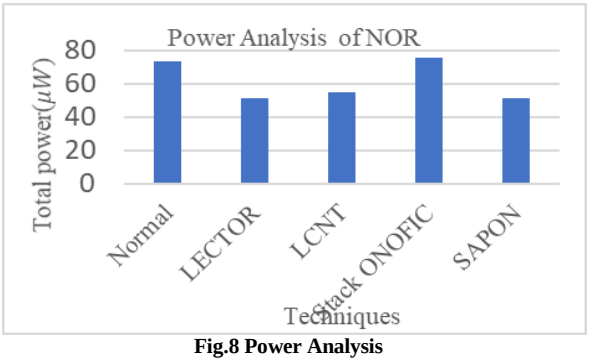

Fig.8 Power Analysis

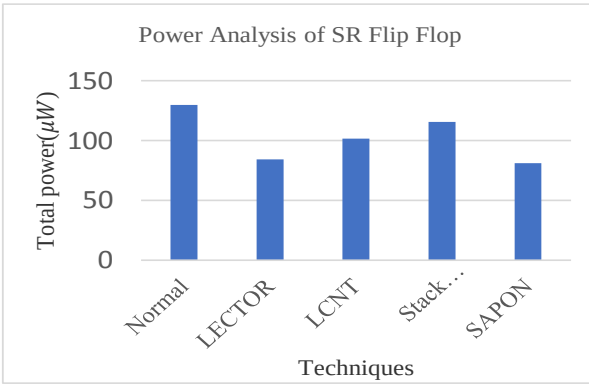

Fig.9 Power Analysis of NOR

CONCLUSION

The conventional methodologies were modified in order to develop a reliable low-power strategy for VLSI in digital systems. For the logic circuit, these techniques are used for low power consumption. Compare to all technique the SAP0N techniques gives greater contribution to 1ow power, which in turn results in energy savings and improved performance. Since we were able to reduce power consumption in basic logic gates by utilizing SAP0N approaches, one can do the same in combinational circuits that are formed from basic gates.

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Conflict of Interest: None

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