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High-Speed 16-bit Carry Bypass Adder Design

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ABSTRACT

Adders are one of the most significant blocks in a logical arithmetic unit. These are employed in a wide range of applications, from incrementing the value of a program variable to high-speed applications such as video-encoding, digital-signal. There are various adders with varying propagation delays. As a result, selecting an efficient adder is critical for system performance. This research compares the latency of several 16 bit adders that are available. The delay of logic gates in 180nm technology has been quantitatively modelled utilizing logical effort. The delay is then utilized to calculate the delay of various adders in Virtuoso Cadence while simulating. Virtuoso Cadence was used to perform functional verification on adders. Each adder's route delay has also been determined. Based on this research, a new carry bypass adder has been developed to reduce propagation delay. The suggested carry bypass adder reduces combinational path latency by 7.2 percent and logical effort delay by 29.5 percent, respectively.

Keywords: Algorithms for 16-bit adders, logical effort, propagation delay, carry skip adder

INTRODUCTION

Adders are circuits that perform numerical addition. They are the fundamental building blocks of arithmetic logic units (ALU). We can add, remove (using one's complement or two's complement), and even multiply using adders as multiplication is simply repetitive summation. These are found in practically every ALU. For the best system performance, a combination of adders is frequently utilised. They are also useful in DSPs that use Multiply-And-Accumulate. It is a critical factor in deciding a DSP's performance. As a result, we require adders with shorter propagation delays and lower power consumption. There are numerous adders, such as the ripple carry adder [1, 2], the carry look ahead adder [3, 4], and so on.
Delay is a key component in determining an adder's performance. The delay of an adder is determined by the logic gate employed in the algorithm's implementation.
The gate-delay is determined by the algorithm it implements, as well as the output load and the number of inputs [3]. The technique of logical-effort could be used to calculate the delays of various logic-gates. These values can then be utilized to compute the propagation-delays of various adders.
In [6,] Bhavani Koyada analysed prevailing 4-bit adders in terms of Xilinx latency. Anacan et al. [5] performed work identical to that described in the paper, comparing different eight-bit parallel adders which were utilised by EDA resources and logical-effort.
This paper investigates and analyses various 16 bit adders in relation to propagation-delay. Aside from the delay achieved from Cadence simulation, an analytical modeling of the propagation-delay of the logic gates employed in this adder was too performed. In addition, new adder topologies with low latency have been proposed based on this research. The first section of the study discusses information on commonly used adders. Section II discusses the method for simulating adders. Sections III and IV

discuss the simulation results of prevailing adders as well as the new adders proposed based on simulation findings. Section V contrasts the new adders with their forefathers. Section VI summarises the findings.

For a long time, many adders such as ripple carry adder [1, 2], carry look-ahead (CLA) adder [3, 4], carry select adder [7] and carry skip adder [5, 6] have been in use. Four complete adders are used in a 4-bit ripple-carry adder (RCA). A half adder can be employed if there is no carry in the first stage. As a result, three full adders and one-half adder are required. The first adder's carry out is the second block's carry in, and so on. As a result, there is a ripple effect of carry, resulting in increased delay. There is no ripple of carry in carry look ahead adder. Any bit's sum and carry can be represented in the form of original carry input. This concept is employed by the carry look ahead adder. If the propagate signal P (the XOR operation of the inputs) is logic-1, the internal carry is not propagated. Instead, the output carry is the input carry.

Logical effort became an excellent tool for locating delays. The absolute delay, dabs, is given as dabs= d.τ [1] where d is the unitless delay and τ is the delay of a single not gate. The gate-delay of a single NOT-gate changes accordingly as the technology library utilised [1], That is, the propagation delay achieved in 45nm technology will differ from the propagation delay acquired in 180nm technology. The unitless quantity (d) is divided into two components: stage effort (f) and parasitic delay (p). The parasitic delay, (p), remains constant regardless of the output load. Table 1 shows a rough estimate of the delay of various gates. [3]

TABLE I. ESTIMATED PARASITIC DELAY FOR A FEW COMMONLY USED GATES

Gate type	Parasitic delay
Inverter	Pinv
N-input NAND	N.Pinv
N-input NOR	N.Pinv
N-Way MUX	2N.Pinv
XOR, XNOR	4Pinv

A unit inverter's parasitic delay (Pinv) is considered to be one[4]. Stage-effort (f), is again subdivided into electrical effort (h) and logical effort (g). The logical-effort (g) simulates the influence of the gate's logic on delay. The electrical effort is determined by the load. (2) f=gh d=f+p [4]. The logical-effort is the ratio of a given gate's input capacitance to that of an inverter capable of generating the same output current (and hence is a constant for a particular class of gate and can be described as capturing the intrinsic properties of the gate). The logical effort for an inverter is 1, 1.33 for a NAND gate with two inputs, 1.66 for a NAND gate with three inputs, 1.66 for a NOR gate with two inputs, and 2.33 for a NOR gate with three inputs, as shown in Figure 1. All gate's logical effort may be computed in the same way. Table II summarises everything.

TABLE II. LOGICAL EFFORT OF SOME GATES

Type of Gate	Total number of inputs					
	1	2	3	4	5	n
NOT gate	1					
N-input NAND		1.33	1.67	2	2.33	(n+2)/3
N-input NOR		1.67	2.33	3	3.67	(2n+1)/3
N-Way MUX		2	2	2	2	2
XOR, X-NOR		4	12	32		

1.1 METHODOLOGY

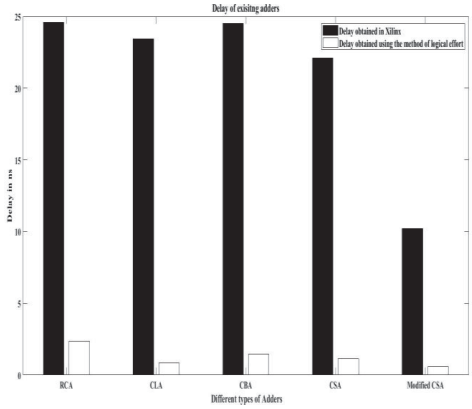
Adder circuits are constructed from various gates. The approach described below is used to simulate and contrast the delays of various adders: First, the approach of logical effort is used to determine delays for distinct gates in a circuit. For the sake of simplicity, all gates are assumed to have homogeneous output loads. The unitless delay is then multiplied by the single inverter delay in 180 nm technology [3]. While simulating in Virtuoso Cadence, the computed delays for a specific gate are utilized as the delay of the associated gate in adders. The worst-case latency may be calculated by supplying different input combinations.

1.2 SIMULATION STUDY OF EXISTING ADDERS

There have been simulations of 16-bit adders such as carry-bypass adder, carry-select adder, ripple carry adder, carry look-ahead adder, Carry select adder with low power and less area [8], (enhanced CSA). Luca Pilato used a CMOS 180 nm

technology library to evaluate several 16 bit adders at 1.8V [8]. The simulated result differs from the work done in [8], which could be owing to an estimation made while determining logical-effort. As demonstrated in Figure. 1, the carry look ahead adder has the shortest propagation-delay and the ripple carry adder has the longest propagation-delay. A 16-bit carry look-ahead adder requires more sophisticated circuitry than a 16-bit ripple carry adder

Figure. 1. The graphical depiction of delay obtained using the logical effort method and Vivado Xilinx 2021.



2. PROPOSED ADDER- CLA-Based Carry Bypass Adder

To speed up the operation, the suggested carry-bypass summer employs a carry look-ahead block rather than a ripple-carry summer. This is significantly faster than the traditional bypass adder since carry-rippling may be bypassed. Figure 2 depicts the suggested adder's block diagram.

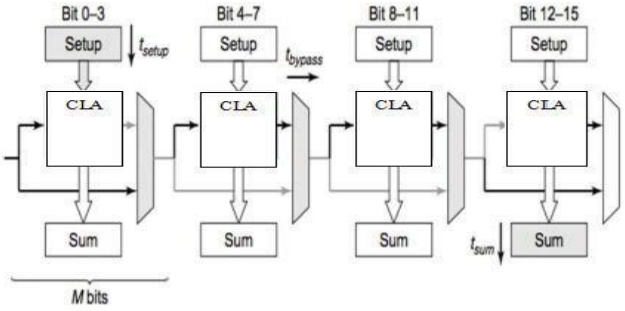


Figure. 2. Proposed Carry-Bypass Adder

3. SCHEMATIC OF PROPOSED ADDER

The schematic of 16-bit proposed carry bypass adder has been realised in virtuoso cadence from the transistor level and the symbols has been created and interconnected as shown in Figure.3.

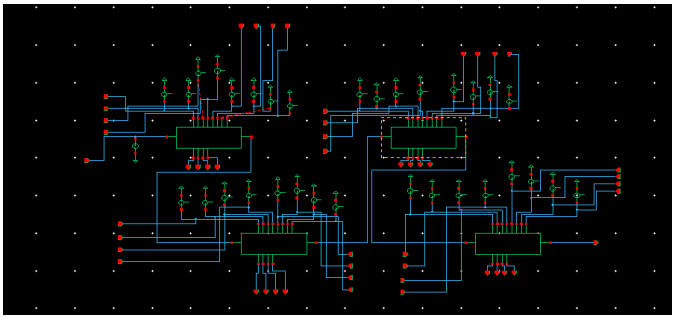


Figure. 3. 16-bit optimised Carry Bypass adder schematic using CLA

4. RESULTS AND SIMULATION

The Verilog code is developed and RTL based simulation has been carried out using Vivado Xilinx 2021.2 and its functional verification is done as shown in Figure.4.

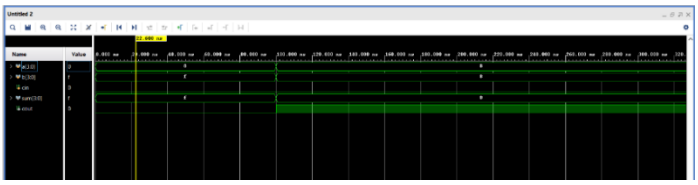


Figure. 4. Simulation waveform for Modified Carry-Bypass Adder in Vivado Xilinx.

The transistor-level analysis of modified carry bypass adder is performed in Virtuoso Cadence and the waveforms generated using transient analysis is shown in Figure.5.

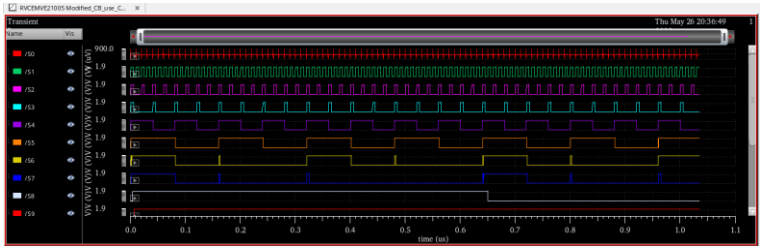


Figure. 5. Transient Analysis of Modified Carry Bypass Adder in Virtuoso Cadence.

The Synthesis of the design is also carried out using genus tool available in virtuoso cadence to calculate various parameters such as power, delay and area as shown in Figure.6.

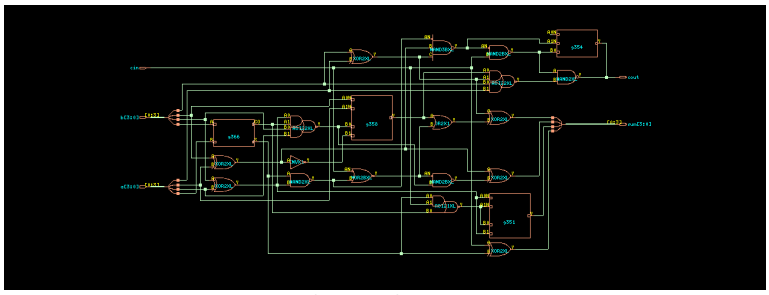


Figure. 6. Synthesized Design for Modified Carry-Bypass Adder using genus

5. COMPARISON OF EXISTING AND OPTIMISED ADDERS

The power and delay obtained by synthesizing already existing adders and optimised adders in Virtuoso Cadence are shown in table 3.

Table III. table of power and delays obtained in Virtuoso Cadence for various Adders

Types of Adders	Delay (in ns)	Power (in µW)
Existing Carry-Bypass Adder	1.408	15.4
Optimised Carry-Bypass Adder	1.306	17.5

6. CONCLUSION

Logical-effort may be used to determine propagation-latency, which in turn can then be used to make a comparison between various adders. Although there may be slight differences from the actual latency [9], the basic pattern may be seen. The ripple-carry adder has the longest propagation-delay. This was taken into account when creating new adders. Carry look-ahead adder has replaced ripple-carry adder in carry-bypass adder. Using Virtuoso Cadence, the adders developed by modifying the carry bypass adder exhibit a 7.2 percent reduction in latency when compared to the standard adder.

Acknowledgement: None

Conflict of Interest: None

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