International Journal of Research and Review
Vol. 9; Issue: 11; November 2022
Website: www.ijrrjournal.com
Research Paper *E-ISSN: 2349-9788; P-ISSN: 2454-2237*

Design of Two stage OTA with Optimised Compensation Capacitance

Pruthvi D[1], Dr. Kiran V[2]

[1]Student, Department of ECE, RV College of Engineering, Bengaluru, India
[2]Associate Professor, Department of ECE, RV College of Engineering, Bengaluru, India

Corresponding Author: Pruthvi D

DOI: https://doi.org/10.52403/ijrr.20221109

ABSTRACT

A two-stage operational transconductance amplifier is constructed and compared between 45nm and 180nm CMOS technology in this paper. To find the best design, the suggested operational amplifier is examined across a number of distinct parameters. With a supply voltage of 1.8V, it reaches a maximum gain of about 66 dB and a phase margin of 82°. A Cadence Virtuoso-based circuit simulator has been used to construct the suggested operational amplifier and the comparison is done.

Keywords: OTA, Miller coupling capacitance, cadence virtuoso, Gain, output swing, power dissipation.

INTRODUCTION

Millions and millions of transistors are presently crammed onto a single die at the evolutionary stage of VLSI technology. The evolution in the field of mixed signal research is significant as a result of analogue and digital functionality in IC designs. The solitary major foundation for implementing the systems that are based on mixed signals i.e., both analog and digital is complementary metal-oxide semiconductor technology, or the CMOS. Because it offers power efficiency, increased density compared to digital systems, and effective integration with diverse analogue system components.

Design and execution of portable gadgets are receiving a lot of attention because of how widely used they are in industry. When technology is downsized, MOSFET cannot operate below the threshold voltage while operation. A crucial component of modelling with analogue mixed signal (AMS) circuits is achieving low power and low voltage functioning. One important strategy that results in low power levels and hence lowers power consumption is regulating the voltage level. The transistor pitch has grown to a size of 2 nm due to scaling the technology node to an extent. Since digital circuits are regular and distinct, computer-based design models can help with proper integration.

On the other hand, because analogue circuit-based models are sophisticated, it is usually preferable to construct them theoretically in order to attain the lowest possible error margin. Higher productivity is attained with fewer errors. The correctness of an analogue circuit depends on factors including manual computations, a non-converging solution space, and long-term product time reliability. The operational amplifier is the key design element in every analogue system. The goal of an OpAmp is to achieve the highest open loop gain feasible in order to integrate feedback concepts and create a more stable system.

LITERATURE REVIEW

An integrated circuit (IC) that functions as a voltage amplifier is known as an operational

amplifier (or an op-amp). There is a differential feed on an op-amp. It therefore has 2 inputs with polarity opposites.[1][2] The output voltage of an op-amp is substantially larger than that of the input signals due to its single output and extremely high gain.

A DC coupled large amplitude digital voltage amplifier which has a differential input and a single ended output is known as an operational transconductance amplifier (called as op amp)[3]. An op-amp will generate an output voltage that is usually many times greater than the gap among its input terminals. The first digital computers used op amp for the basic computations that were of different topology[4].

By stacking so at load and supply side, single stage Op-Amps provide a significant amount of gains, while this also restricts the output fluctuations. However, there are a wide range of uses for these circuits. We choose two-stage opamps for high-end operations since the first stage mostly adds to gain while the second stage, while it also boosts gain, primarily focuses on boosting swing[5][6].

There are no restrictions on how an amplifier can be chosen for each stage. Both the first stage and the second level can use different amplifiers. In order to enable the widest possible output swings, the second stage is typically set up as the common source stage. A differential amp is taken into consideration for the initial stage and its swing is extended by attaching a Common-source PMOS amplifier[7].

By replacing the load in a cascode style, the gain of the first stage can also be enhanced. As gm2*(r02 || r04) and gm7*(r06 || r07), in both, can be used to express the gains of the initial and second stages. As each level results in the inclusion of a pole, the main issue with a two-stage opamp is that another pole is added, which makes stability unassured. For this reason, opamps with multiple stages are not frequently employed. Harmonic provides lower can be used to provide the answer to this problem[8].

Operational amplifiers can be characterised as either buffered or unbuffered. The output resistance of unbuffered operational amplifiers is often very large. To distinguish the difference between maximum output resistance and a low output resistance, use the terms buffered and unbuffered. Operational transconductance amplifiers are characterized as unbuffered operational amplifiers because of their high output resistance. Due to their low resistance, voltage amplifiers fall within the category of buffered Op-Amps.

The primary objective of an Op Amp is to achieve the highest open loop gain possible for the implementation of the feedback concepts and create a more stable system. To achieve high gain with stability, most of the op amp circuit models are constructed based on multistage nodes. The majority of circuit designs used today are two stage concepts. Utilizing such a developed model will lead to more reliable execution and simple eradication of load inequalities between construction process. Single stage Op-Amps are used to convert voltage to current, which minimizes the system gain and decreases the amount of amplification[9].

Cascading is one way to make up for the losses, however it will cause distortion from the huge output voltage swings. Using cascode Op-Amp, that can generate higher gain and significantly stable designs, was therefore chosen as the best choice. Given the previously mentioned need for high gain in real situations, designs almost always have more than two stages to allow high gain and larger output swings[10]. Cascode amplifiers use their first stage for high gain and their second stage for large output swings

DESIGN METHDOLOGY

A. Saturation region of operation

The design can work at supply voltage and bias currents because the transistor in the subthreshold region operates below the threshold voltage.[8] provides the equation

for the drain current (I_D) in the switching frequency zone.

$$I_D = \frac{W}{L} I_0 \exp\frac{V_{GS} - V_{th}}{mV_T}(1 - \exp\frac{-V_{DS}}{V_T})$$
$$\approx \frac{W}{L} I_0 \exp\frac{V_{GS} - V_{th}}{mV_T}(when: V_{DS} > 3V_T) \quad (1)$$

$V_T = k_BT/q$ that is equal to 26 mV is the specific voltage at the room temperature, where W/L is the tr aspect ratio, V_{GS} and V_{DS} are the gate(G) to source(S) voltage and drain(D) to source(S) voltage, respectively, V_{th} is the threshold voltage, k_B is the Boltzmann constant at the room temperature, T is the absolute temperature or the specific temperature, and q is the charge, m is the sub threshold or the saturation slope parameter. These are technology dependent and typically between the value 1 to 2, and I_0 is the parameter that depends on temperature(T).

According to the equation(1), the connection between the output current(I_o) and the input voltage(V_{in}) is exponential instead of quadratic relation, since it occurs in strong inversion region. By increasing the transconductance of the MOSFET, this raises its gain and gives it properties resembling those of a BJT.

The threshold voltage V_{th} is given by [9] after drain-induced barrier lowering (DIBL) and body effects are taken into account.

$V_{th} = V_{th0} - \lambda_D V_{DS} - \lambda_B V_{BS}$ with λD and $\lambda B > 0$ (2)

where V_{BS} is the body(B) to source(S) voltage, V_{th0} is the room temperature threshold voltage (for V_{BS} = 0V), and D and B are the coefficients of the body effect and DIBL [10]. (1) and (2) can be used to derive the equation for transconductance gm [11].

$$g_m = \frac{I_D}{mV_T}$$
$$\frac{W}{L} = \frac{I_D}{I_0} \exp\frac{V_{TH} - V_{GS}}{mV_T} \quad (3)$$

B. Design Methodology of two stage operational amplifier

In Figure 2, a two-stage Miller-compensated Op Amp is shown with its transistor-level setup (VBS = 0V), without any specific MOSFET body terminal exploitation method in use. The architecture of the suggested circuit is built to boost the input data between 2 steps, the first of which is the differential step and the second of which is the gain stage. In the proposed system, all MOSFETs work in the saturation region.

Table II displays the design based objectives that are specified for the two stage Operational Amplifier, and these parameters were selected in accordance with the viability and practicality of biomedical applications. A Vdd value of 1.8V is used for supply voltages. The Vth value was calculated by using equation and the constants from Table I given above.

Table II: DESIGN GOALS

Parameters	Specified Values
Supply voltage	1.8 V
Power dissipation	< 300 mW
Small signal gain	>60dB
Slew rate	20 V/ µs

Each MOSFET's W/L values were determined using Equation (3), and the drain current(I_D) for each MOSFET was calculated using the maximum permissible power dissipation and V_{dd} value. After doing a DC analysis on the 1st stage i.e., the differential amplifier part of the op amp, the DC bias voltage V_{REF1} is given according to the gain specifications once the proper aspect ratios for all of the MOSFETs had been established. After that, VREF2 was adjusted to provide the appropriate gain for the entire amplifier.

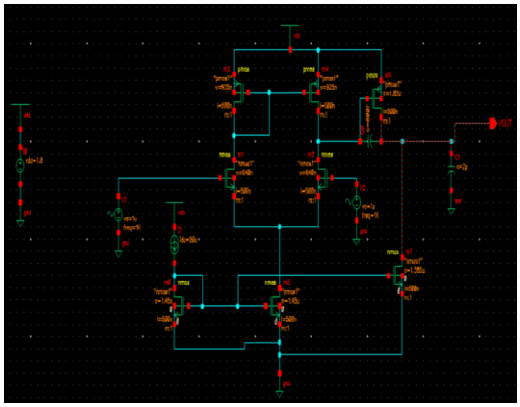

Fig. 2. Schematic circuit of the 180nm based two stage operational amplifier with capacitance compensation

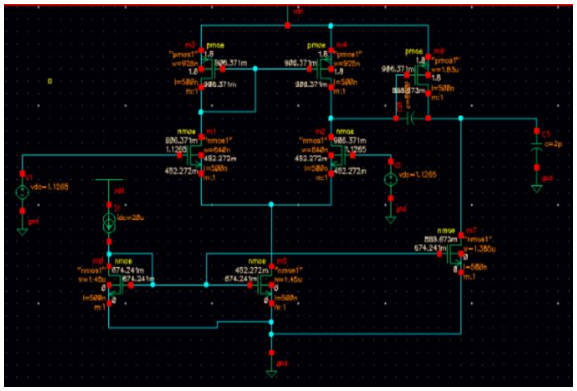

Fig. 3. Schematic circuit of the 45nm based two stage operational amplifier with capacitance compensation

C. Improvement in performance

Practical methods for enhancing the OTA's performance were taken into consideration after the circuit design, aspect ratios and biasing are calculated and fixed. A well-known method for increasing system stability at the appropriate bandwidth is Miller Compensation. To divide the poles and increase Phase Margin at the price of UGB, it entails connecting a capacitor (Cc) in negative feedback at the Unity Gain Bandwidth. The compensation capacitance was discovered utilising the following equation to realize the compensation and then obtain the appropriate UGB.

$$C_C = \frac{g_{m1}}{2\pi UGB}$$

where gm1 is the transconductance of M1 determined using Eqn, and Cc is the compensating capacitor (3). Then, while boosting bandwidth, the compensating resistance was discovered to stabilise the Operational Amplifier and correct the phase margin.

Table III: MOSFET DIMENSIONS AND NETWORK ELEMENTS

Parameter	180nm	45nm
M1,2	640nm	146nm
M3,4	925nm	125nm
M5	1.45µm	935nm
M6	1.83µm	720nm
M7	1.385µm	745nm
CC	800fF	1.2pF
CL	2pF	2pF

SIMULATED

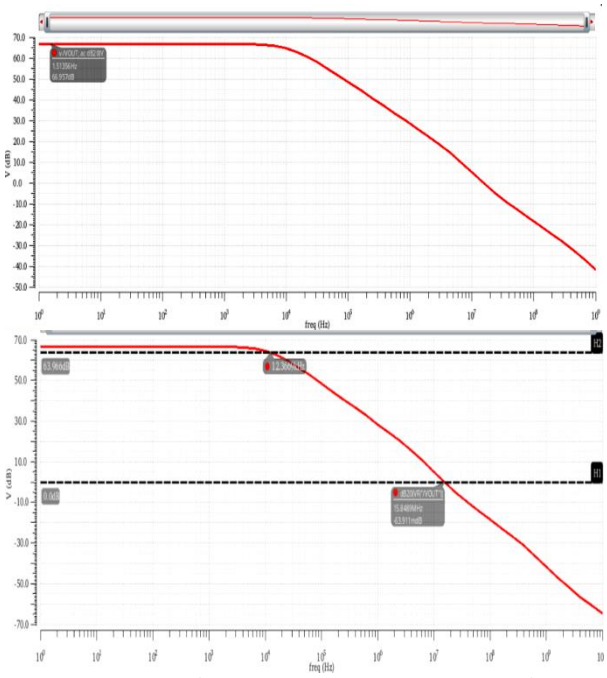

Fig. 4. AC gain plot for the two-stage Operational Amplifier for 180nm and 45 nm technology

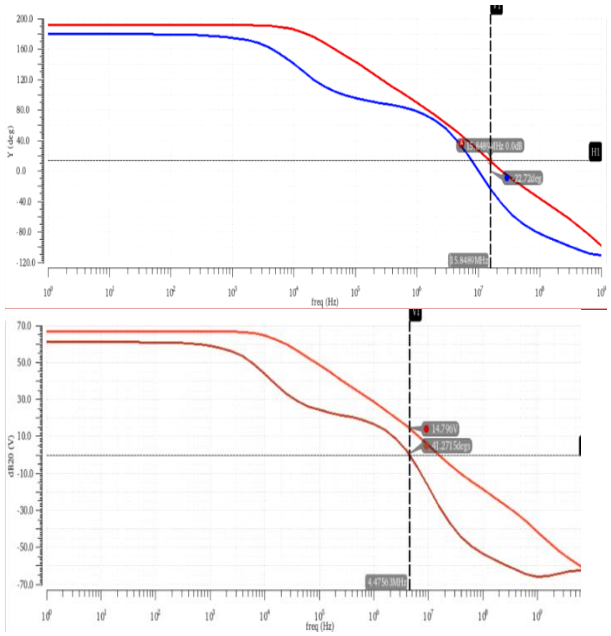

Fig. 5. Phase margin of the two stage Operational Amplifier using the 180nm and 45 nm technology

The Schematic circuit of the 45nm based two stage operational amplifier with capacitance compensation is shown in Fig 3. The frequency response of the open-loop amplifier for each of the three technology nodes is shown in Figure 4. Figure 4 illustrates the 180 nm technology node's dc

gain, which were determined to be 63.95dB. As the node technology was scaled down to 45nm, it was discovered that the values of dc gain at the output and the phase margin are noted to be rising, with 45nm technology exhibiting the best performance, as shown in Fig4. The system's max phase margin is noted.

Table IV displays the simulation results for both the technologies. It was discovered that power consumption was rising as technology scaled, as would be predicted for voltage scaling which is constant. As seen, with a small amount of divergence caused by inevitable ambiguity and estimates in the theoretical calculations, the majority of the parameters fulfil the design objectives of Table II. Both the technologies will offer the high gain and low power consumption[15].

Table IV: SIMULATION RESULTS

Parameter	**180nm**	**45nm**
Phase Margin	-22.72°	-41.27°
DC Gain	63.96 dB	66.95B
Supply voltage	1.8V	1.2V
Power dissipation.	123.92nW	152.6nW
Unity Gain BandWidth	12.374kHz	24.365kHz
C_L	2pF	2pF

In Table V, the listed the key characteristics for each of the three technologies, both with and without Miller compensation, to illustrate the impact of Miller compensation for the suggested configuration.

Table V: EFFECTS OF COUPLING CAPACITANCE

Technology (nm)	**Without the Miller Compensation**		**With Miller Compensation**	
	UGB (kHz)	**Phase Margin(°)**	**UGB (kHz)**	**Phase Margin (°)**
180nm	109.02	-22.72	27.54	63.5
45nm	352.76	-110.8	31.62	76

CONCLUSION

This paper proposed a design methodology for a 1.8V and 1.2V supply voltage, high gain, low power transconductance op-amp. The scaling is done to make sure the smaller circuit was analysed for the suggested OpAmp for the 180nm and 45nm technologies. As the type of technology was scaled down, the patterns predicted by theory were followed, with gains, phase margins, and as well as power rising. According to the two technologies, the 45nm technology node had the finest phase margin (82°), while the 180nm technology node offered the highest gain (66.95dB) and Unity Gain Frequency (24.365 kHz). The suggested design maintained reasonably high gain (about 66.95dB) and low power operation across all technologies while demonstrating enhanced slew rate and Unity Gain Bandwidth in comparison to the results in other studies.

Acknowledgement: None

Conflict of Interest: None

REFERENCES

1. M. H. Hamzah, A. B. Jambek and U. Hashim, "Design and analysis of a two-stage CMOS op-amp using Silterra's 0.13 µm technology," 2014 IEEE Symposium on Computer Applications and Industrial Electronics (ISCAIE), 2014, pp. 55-59, doi: 10.1109/ISCAIE.2014.7010209.
2. Sadeqi, J. Rahmani, S. Habibifar, Design Method for Two-Stage CMOS Operational Amplifier Applying
3. Load/Miller Capacitor Compensation, Computational Research Progress in Applied Science & Engineering, CRPASE: Transactions of Electrical, Electronic and Computer Engineering, 2020,153–162.
4. R. Nagulapalli, K. Hayatleh, S. Barker and B. N. K. Reddy, "A two-stage opamp frequency Compensation technique by splitting the 2nd stage," 2020 11th International Conference on Computing, Communication and Networking Technologies (ICCCNT), 2020, pp. 1-5.
5. N. M. Laskar, S. Nath, S. Chanda and K. L. Baishnab, "A high gain, low power two stage OpAmp using self cascoding technique for Low Frequency Application," 2017 Devices for Integrated Circuit (DevIC), 2017, pp. 267-271, doi: 10.1109/DEVIC.2017.8073949.
6. Yadav and S. Prasad, "Low Voltage Low Power Sub-threshold Operational Amplifier in 180nm CMOS", 2017 Third international conference on sensing signal processing and security (ICSSS), pp. 35-38, 2017.

7. L.H. C. Ferreira, T. C. Pimenta and R. L. Moreno, "An Ultra-Low-Voltage Ultra-Low-Power CMOS Miller OTA With Rail-to-Rail Input/Output Swing", IEEE transactions on circuits and systems, vol. 54, no. 10, pp. 843-847, 2017.
8. S. Nitundil, N. Singh, R. Balaji and P. Arora, "Design and Comparative analysis of a Two-Stage Ultra-Low-Power Subthreshold Operational Amplifier in 180nm 90nm and 45nm technology", 2021 Devices for Integrated Circuit (DevIC), pp. 36-40, May 2021.
9. N. R. Jangam and S. Ajmera, "Design and Implementation of Ultra low power CMOS based Operational Trans-conductance Amplifier (OTA) for Biomedical Applications", 2021 2nd International Conference for Emerging Technology (INCET), pp. 1-4, May 2021.
10. V. Mythry and J. Moni, "A 76db 828nv/-VHz Low Noise Bio Signal OTA For Neural Signal Recording Applications", International Journal of Engineering and Technology (UAE), vol. 7, pp. 48-53, Jun. 2018.
11. Yadav and S. Prasad, "Low Voltage Low Power Sub-threshold Operational Amplifier in 180nm CMOS", 2017 Third international conference on sensing signal processing and security (ICSSS), pp. 35-38, 2017.
12. L.H. C. Ferreira, T. C. Pimenta and R. L. Moreno, "An Ultra-Low-Voltage Ultra-Low-Power CMOS Miller OTA With Rail-to-Rail Input/Output Swing", IEEE transactions on circuits and systems, vol. 54, no. 10, pp. 843-847, 2017.
13. S. Nitundil, N. Singh, R. Balaji and P. Arora, "Design and Comparative analysis of a Two-Stage Ultra-Low-Power Subthreshold Operational Amplifier in 180nm 90nm and 45nm technology", 2021 Devices for Integrated Circuit (DevIC), pp. 36-40, May 2021.
14. N. R. Jangam and S. Ajmera, "Design and Implementation of Ultra low power CMOS based Operational Trans-conductance Amplifier (OTA) for Biomedical Applications", 2021 2nd International Conference for Emerging Technology (INCET), pp. 1-4, May 2021.
15. V. Mythry and J. Moni, "A 76db 828nv/-VHz Low Noise Bio Signal OTA For Neural Signal Recording Applications", International Journal of Engineering and Technology (UAE), vol. 7, pp. 48-53, Jun. 2018.
16. G. Palmisano, G. Palumbo and S. Pennisi, "Design Procedure for Two-Stage CMOS Transconductance Operational Amplifiers : A Tutorial", Analog Integrated Circuits and Signal Processing, vol. 27, no. 3, pp. 179-189, 2021.
17. H. S. Raghav, B. P. Singh and S. Maheshwari, "Design of low voltage OTA for bio-medical application", 2013 Annual International Conference on Emerging Research Areas and 2013 International Conference on Microelectronics Communications and Renewable Energy, pp. 1-5, Jun. 2013.
18. S. H. Hesari, A. He, Dayatip Our, S. Aslanzadeh and S. K. Islam, "Ultra Low-Power OTA for Biomedical Applications", 2019 United States National Committee of URSI National Radio Science Meeting (USNC-URSI NRSM), pp. 1-2, Jan. 2019.
19. K. Garradhi, N. Hassen and K. Besbes, "Low-voltage and low-power OTA using source-degeneration technique and its application in Gm-C filter", 2016 11 th International Design Test Symposium (IDT), pp. 221-226, Dec. 2016.
20. S. Bandyopadhyay, D. Mukherjee and R. Chatterjee, "Design Of Two Stage CMOS Operational Amplifier in 180nm Technology With Low Power and High CMRR", International Journal of Recent Trends in Engineering & Technology, vol. 11, Jun. 2014.

How to cite this article: Pruthvi D, Kiran V. Design of two stage OTA with optimised compensation capacitance. *International Journal of Research and Review*. 2022; 9(11): 60-65.
DOI: *https://doi.org/10.52403/ijrr.20221109*

******