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I2C Master Scan Chain Insertion and Functional Coverage

Nagendra Prasad N[1], Dr. Kiran V[2]

[1,2]Department of Electronics and Communication, R.V College of Engineering, VTU University, Bangalore, India

Corresponding Author: Nagendra Prasad N

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ABSTRACT

I2C is a serial, bidirectional bus for communication that Philips Semiconductors created. only two bus lines are needed a (SDA) serial data line and a (SCL) serial clock line. With the addition of scan chains, a method for I2C Bus testing has been implemented in this study. In order to achieve the necessary requirements, the number of scan chain insertions is predetermined. The coverage of the Functions is also performed to verify the test bench.

Keywords: I2C, Scan Chain, Coverage, Testing, Design for test

INTRODUCTION

I2C buses are becoming more and more popular for a variety of factors. Compared to other serial communication-based protocols, its operation is easier because it only requires two wires to interface devices. The I2C protocol includes a variety of features, including the capacity to handle numerous masters, a large number of slaves, and connections utilizing just two wires and the functions Start and Stop conditions, as well as reading and writing activities. Low-speed applications are better suited for I2C. But because of recent developments, I2C can now move data at speeds of up to 3.4Mbps.[1][2]

Scan chain is a design for testing techniques. By offering a straightforward method to set and analyze each flip-flop, the key objective is to accelerate testing and simplify the process. Scanning chains are far superior because of their great controllability and observability.

Design for test (DFT), and in particular the implementation of scan test, are essential components of the design process for any contemporary chip design with a significant amount of logic. DFT helps to decrease the complexity of testing sequential circuits. The fundamental idea behind a scan test is to chain together memory components like flip-flops and latches so that switching between scan chains allows the DUT's states to be controlled and observed.

LITERATURE REVIEW

This research proposes a novel bit-based scan chain reordering technique. The care bits are merged using the suggested technique towards the beginning of scan chains. A decrease in scan cell switching has been realized, ensuring scan shift operations. Test power consumption is decreased by the suggested scan chain reordering technique. [9].

This work proposes a safe scan architecture that keeps the debuggability of the scan dump while enhancing scan design security using a skew-based lock and key. The suggested architecture combines the physical information into a lock-and-key system to create an imperceptible defense against the attacker. The paper improves the circuit's security and protects it from scan dumps.[10].

Two innovative and effective Scan flipflop designs that use less power, space, and delay

have been applied in this article. The two novel Scan flip-flop designs, a modified Transmission Gate-based Scan flip-flop and a Gate Diffusion Input-based D flip-flop, were created in Cadence Virtuoso. Speed was noticed to be faster in functional and test modes.[11].

MATERIALS & METHODS

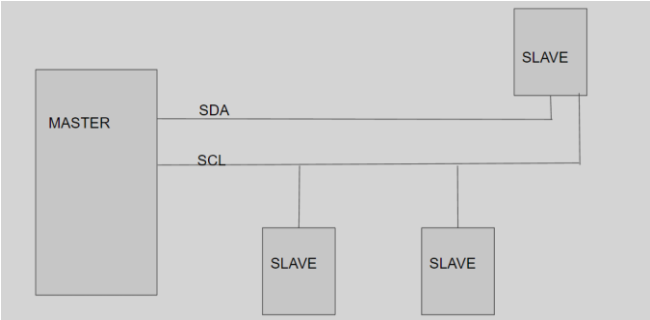

Fig 3.1 I2C basic implementation

A. I2C Methodology

The fundamental I2c architecture, which consists of a single master and a single slave, has been developed as shown in the fig3.1.

8-bit blocks of information are transferred, and the configuration can use a multi-master technique.

When the slave device cannot accept any more data, a unique technique called clock stretching is used. This causes the SCL signal to go low, which causes the master to be disabled and raises the CLK signal. Because the wires are connected in an AND fashion, the master signal must wait until the slave releases the SCL line to ensure that it is prepared to send the next bit before raising the CLK signal.[2]

It follows a simple process for validation of data transfer

Using two shared bus lines, any of the devices on the I2C network can be controlled.

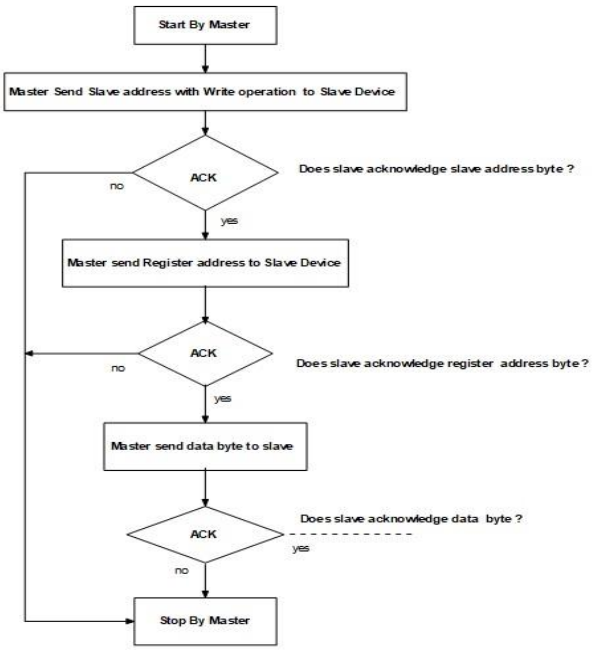

Fig 3.2 I2C flow chart

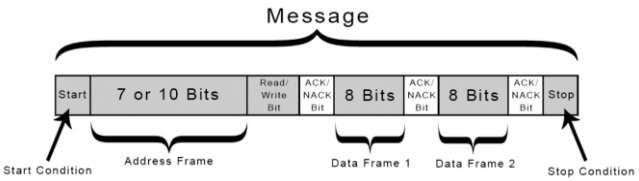

Fig 3.3 I2C data frame

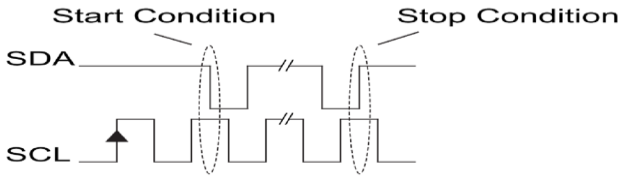

Fig 3.4 I2C start and stop condition

As shown in the fig 3.4 , the start condition is indicated by the pulling the SDA line down when the scl line has high voltage and to indicate the stop the SDA line is pulled high when the scl line is high.[4] [5]

ADDRESS

This is the frame that follows the start bit right away. Each slave connected to the master bit receives the address of the slave with which it must talk. The slave bit then compares its own address to the slave's address that the master sent. A low-voltage ACK signal is sent to the master signal when both addresses match. The slave is idle and the serial data line is HIGH when the addresses of the two devices do not match.

Read/Write

The master is sending data to the slave when the Read/Write signal reads "1," yet the master is receiving data from the slave signal when the read/write signal reads "0."

ACK/NACK

Each message frame's following bit is the acknowledge/no-acknowledgment bit. When data or an address is successfully sent, the receiver device sends the ACK signal back to the sender.

B. Scan Chain Insertion

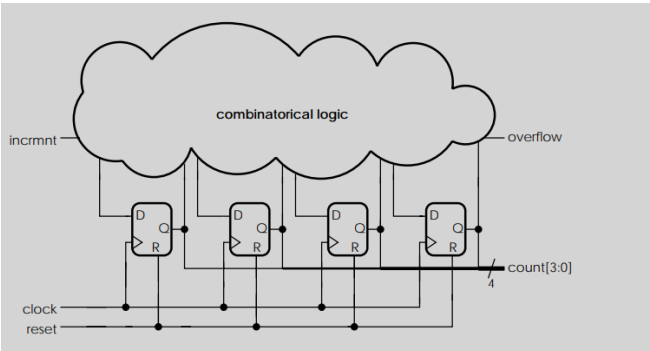

Fig 3.4 Scan Chain Insertion

Scan chain's simplest building block are (SFF) scan flip-flops. A mux is located at the input of a scan flip-flop on the inside. The SE (enable signal for mux) controls whether D (functional input) or SI (test input) will arrive at the flip-output when the active clock edge reaches Clk.

In the testing design, the scan flip-flops are used in place of every flip-flop (for a complete scan design). An interconnected

scan chain is created using the scan flip-flops.
When the design is in test timing mode and the SE (test enable signal) is activated, the scan chain functions as a shift register. The scan input port is connected to the first flip-flop in the scan chain, and the scan output port is connected to the last flip-flop in the scan chain. Partial scan designs are those in which some flip-flops are omitted from the scan-flop conversion process on purpose. Full scanning a design increases its testability for manufacturing flaws at the expense of complexity, area, and power.[5][8]

The scan chain operation is divided into three phases:

Scan In Test patterns are loaded in Scan flops when the testing mode is activated.
Capture Objective: The pattern during test mode is recorded while the design is maintained in functioning mode.

Scan Out Goal: Test pattern outputs are discharged and the design is returned to testing mode (Sometimes, this procedure starts the Scan In injection of the next test pattern at the same time.)

Since stuck-at testing is performed at a reduced frequency, just a single capture pulse of the clock is required. The Path Delay or Transition fault tests are carried out at functional speed, with the design placed in the function timing mode (at speed testing).

RESULT

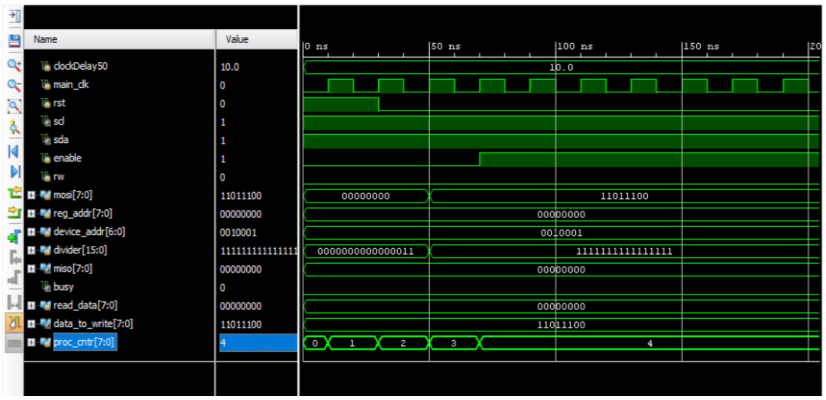

Fig 4.1 Master operation

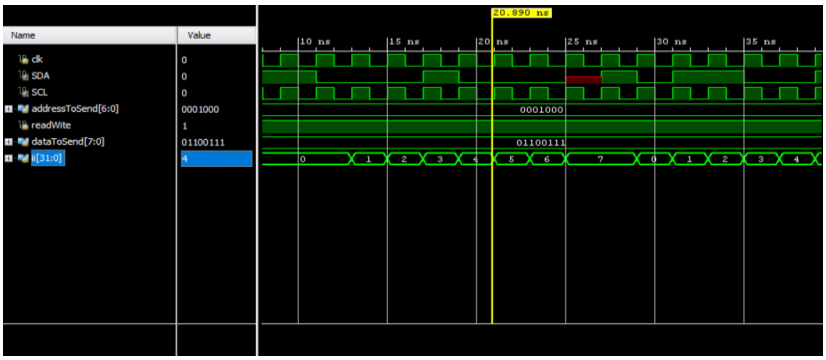

Fig 4.2 Slave operation

I2c master and slave operations are shown as above.
The corresponding synthesis of the I2c master is as shown in the image without the scan chain. (Fig4.3)
Fig 4.4 and Fig 4.5 indicate the synthesis of the I2c master with 20 and 50 scan chains respectively with synthesis optimizations.

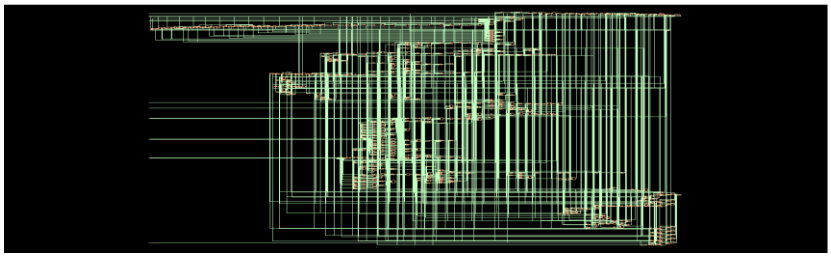

Fig 4.3 Slave operation

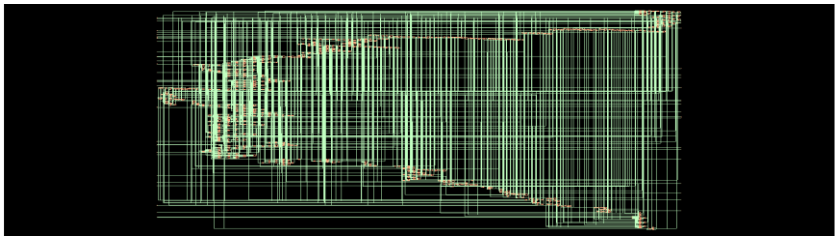

Fig 4.4 Slave operation

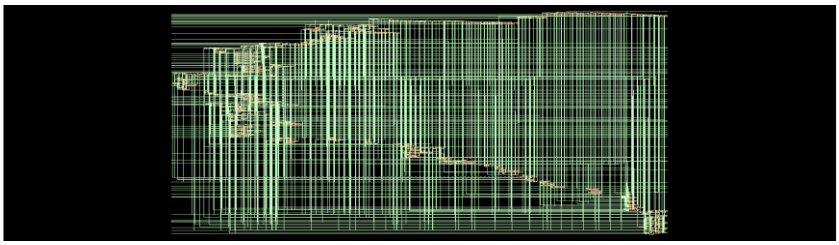

Fig 4.5 Slave operation

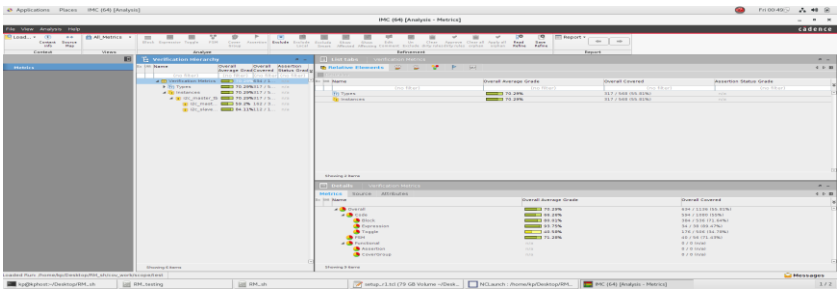

Fig 4.6 Functional code coverage

I2C master of the scan chains is illustrated as follows.
The number of scan chains and power is illustrated in the following table 4.1 as shown there is a rise in the power consumption as the number of scan chains increases.

sl no	Attribute	time slack	Power
1	0	98.868us	11.817uW
2	20	99.212us	36.734uW
3	50	99.214us	37.501uW

Table 4.1 relation between power and scan chains

sl no	number of scan chain	Coverage
1	Code	66.61
2	Block	80.01
3	Expression	93.75
4	Toggle	40.58
5	FSM	71.28
6	Overall	70.29

Table 4.2 Coverage Obtained

DISCUSSION

A method for the addition of scan chain in the I2C module has been performed. The addition of Scan chain made the testing process simple and faster without much overhead.

An analysis of the code coverage of the testbench is also checked to ensure that the functionality is verified.

CONCLUSION

The analysis of the power consumption and the timing slacks for three different designs with scan chains have been presented. The increase in the timing slack is not much affected by the addition of more number of scan chains indicate that the two modes testing mode and design mode are separate and do not intervene with each other's timing paths. A functional coverage for the corresponding design is also performed to determine the percentage of the coverage and the quality of the testbench.

Acknowledgement: None

Conflict of Interest: None

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