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Design and Implementation of Optimized Reversible 4-Bit Linear Feedback Shift Registers for Computing Applications

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ABSTRACT

Reversible logic has emerged as a major area of research in recent years due to its ability to reduce power dissipation which is the main requirement in the low-power VLSI. Reversible Computing has shown greater impact to have enormous applications in emerging technologies such as Quantum Computing, QCA, Nanotechnology and Low Power VLSI. In this paper, we have realized Optimized Reversible Linear Feedback Shift Registers (LFSR) and have explored it in terms of delay, quantum cost, garbage outputs. We have shown a new reversible realization of Serial Input Serial Output (SISO) and Serial Input Parallel Output (SIPO) registers up to N-bit for the design of LFSR. Proposed circuits have been simulated using Vivado 2016.4 and synthesized by using FPGA Nexys-4 DDR.

Keywords: Reversible Logic, SISO-Serial Input Serial Output, SIPO-Serial Input Parallel Output, Quantum Computing, Reversible LFSR-Linear Feedback Shift Register.

1. INTRODUCTION

The major limitation of technology is power dissipation, which plays a crucial role in digital design in terms of data loss. Hence, reduction of power dissipation remains as an important goal in the VLSI circuit design for many years. Conventionally, digital circuits have been implemented using the basic gates which were irreversible in nature. By using these irreversible logic gates, the circuit life gets reduced as those gates will dissipate more amount of heat. [1] Thus, for every bit of information conventional combinational logic circuits dissipates heat. In 1961, R. Landauer proved that logic computation generates *kTln2* joules of heat energy for every bit of information loss where *k* is Boltzmann's constant and *T* is the absolute temperature of the environment. [2] In order to avoid the data loss, the circuit should build with reversible gates instead of irreversible logic gates, which was stated by C. Bennett in 1973. [3] Reversible logic does not lose information.

Bennett showed that it is possible to have zero dissipation if network is built with reversible gates only. [4] Reversible logic has also found its applications in several technologies; [5-13] such as optical computing, [5] ultra-low power CMOS design,[6] and nanotechnology. [7] Thus, research on reversible logic essential for the development of future technologies. As there is no possibility of feedback in case of, implementing reversible logic using combinational circuits T. Toffoli in 1980 has shown that feedback is allowed in reversible computing. [8] According to his theory, a sequential circuit is reversible if its combinational part is reversible. Most of the recent works focus on optimizing the reversible sequential design in terms of garbage outputs, delay, number of reversible logic gates, quantum cost. Among all the sequential circuits, shift registers are the most prominently used functional devices in

digital system for storing and shifting the multiple bits.

In this paper, we have shown the realization of two shift registers namely, SISO and SIPO for their application in designing optimized LFSR using reversible gates. The paper is organized as follows; Section 2 highlights the basic reversible gates which includes a new MF gate with its quantum representation. Section 3 reveals the design of shift registers with reversible gates. Section 3 also describes the serial input serial output and serial input parallel output, respectively. Section 4 gives the proposed design of reversible LFSR with the simulation results of pulse triggered reversible LFSR. Conclusions are discussed in Section 5.

2. Brief overview of reversible logic gates

2.1. Feynman Gate

The controlled NOT gate (CNOT) is also known as Feynman gate. Every linear reversible function can be built by composing only 2*2 Feynman gate and inverters as shown in Fig 1. [14] Here controlling input is A and the controlled input is B; P and Q are the two outputs of the gate. The corresponding quantum cost is about 1. It is used to overcome the fan-out problem since it can be used for copying the information.

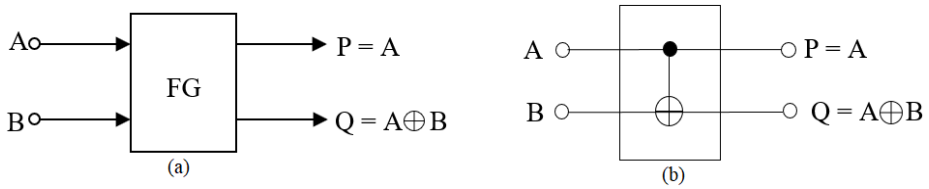

Fig. 1. (a) Feynman gate and (b) Quantum implementation of Feynman Gate.

2.2. Toffoli Gate

It is a universal reversible logic gate, i.e., any reversible circuit can be constructed from Toffoli as shown in Fig 2. [8] The inputs and outputs can be mapped as (A, B, C) to (P = A, Q = B, R = A.B⊕C), where the inputs are A, B, C and the outputs of a Toffoli gate are P, Q, R. Its quantum cost is about 5. It is a controlled-controlled-not gate (CCNOT). It has 3-bit inputs and outputs.

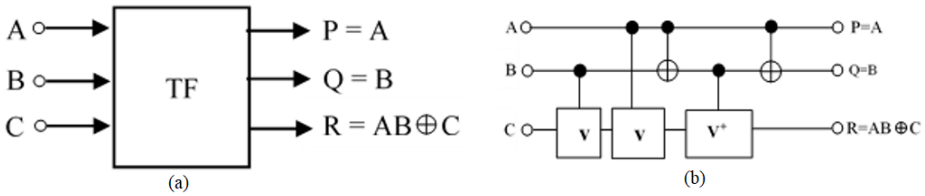

Fig. 2. (a) Toffoli Gate and (b) Quantum implementation of Toffoli Gate.

2.3. Fredkin Gate

It is also termed as a Controlled Swap Gate. Fredkin gate is a 3*3 gate as shown in Fig 3. [15] The Fredkin gate maps inputs (A, B, C) to outputs (P=A, Q = A'B + AC, R = AB + A'C), where the inputs are A,B,C and the outputs are P,Q,R, respectively. The corresponding quantum cost is about 5. Every Boolean function can be built from 3*3 Fredkin Gates. It is conservative and it is its own inverse.

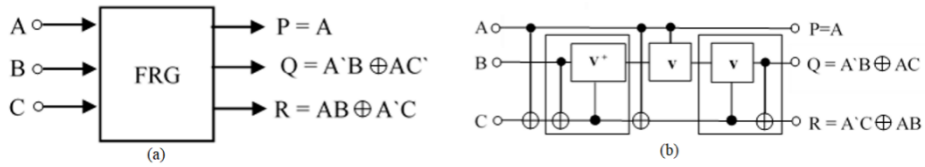

Fig. 3. (a) Fredkin Gate and (b) Quantum implementation of Fredkin Gate.

2.4. Modified Fredkin (MF) Gate

The MF gate is the proposed modified version of 3*3 Fredkin gate with a quantum cost of about 4 as shown in Fig 4, where the inputs are A,B,C and the outputs are P,Q,R, respectively.

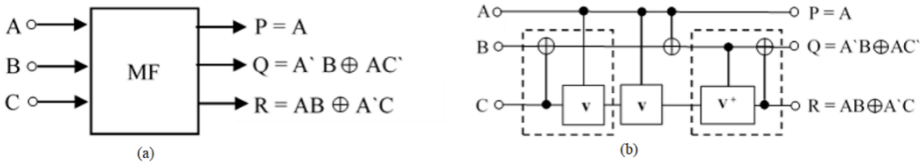

Fig. 4. (a) Modified Fredkin Gate and (b) Quantum implementation of modified Fredkin Gate.

3. Reversible shift register

A flip-flop is a bi-stable electronic circuit that has two stable states and can be used as a single-bit memory device. Combinations of flip-flops are used to store more number of bits, which is termed as Shift Registers. Data can be loaded in two ways i.e., Serial and Parallel Loading, to store the data bits. Data is shifted from one flip-flop to another flip-flop in serial form in case of Serial Loading i.e., one bit at a time upon triggering clock. In parallel Loading, all data bits appear at a time in parallel form upon triggering clock. Serial-in Serial-out and Serial-in Parallel-out are the proposed shift registers in this section. We are using master-slave D flip-flop to design reversible shift register for pulse generation.

3.1. Reversible D flip-flop using Reversible gates

The characteristic equation of reversible D flip-flop can be written as Q^+=D i.e., output is same as input as shown in Fig. 5. The characteristic equation of clock enabled reversible D flip-flop can be written as Q^+=D.E+$\bar{E}$.Q. To avoid fan-out problem, a Feynman gate is used to copy the output.

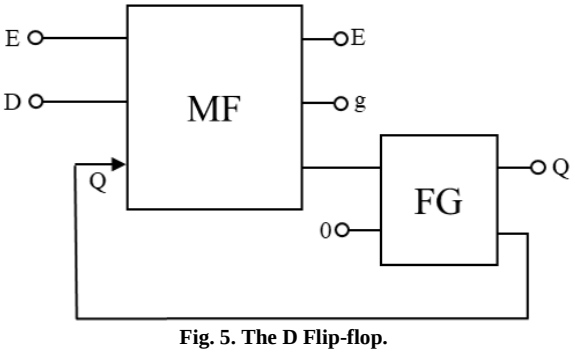

Fig. 5. The D Flip-flop.

Fig. 6 depicts D flip-flop with clock enabled where output Q^+=D for E=1 and output Q^+=Q for E=0 i.e., output remains in its previous state. When D=1 and Q=0, the output of MF logic gate is Q^+=1 (when E=1) which is applied as feedback to Feynman gate.

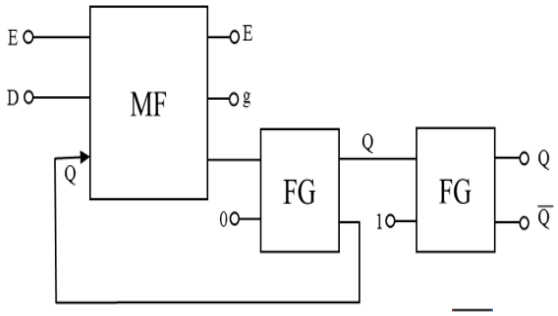

Fig. 6. The D Flip-flop with output Q and $\overline{Q}$.

The proposed Master-Slave configuration of D flip-flop using MF and FG gate are shown in Fig.7-9.

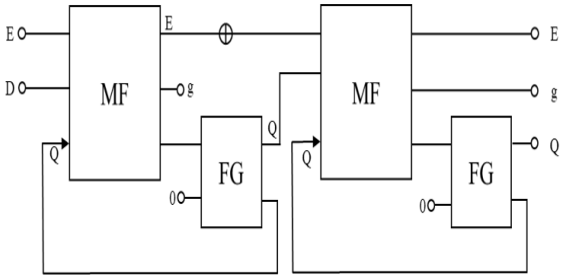

Fig. 7. Master Slave D Flip-flop using MF Gate.

In case of master-slave D flip-flop using MF gate and Feynman gate, a clock inversion exists at the output of slave flip-flop i.e., $\bar{E}$. To use this clock pulse to the next flip-flop in a shift register, we need an extra gate called NOT gate to convert $\bar{E}$ into E. To overcome this problem, we proposed a new architecture of master-slave D flip-flop with MF and Fredkin gate which is shown in

figure that replaces the MF gate in slave flip-flop with Fredkin gate, so that no clock inversion is required and produce same clock pulse as what is applied to its input. To realize registers, this proposed design is used for Master-Slave D flip-flop.

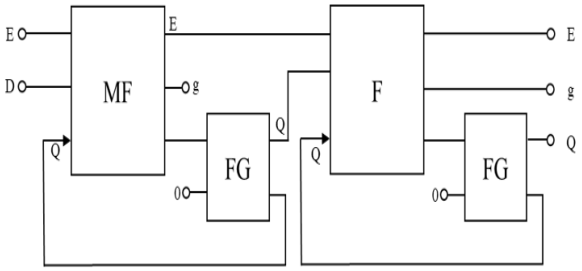

Fig. 8. Master Slave D Flip-flop using MF and Fredkin Gate.

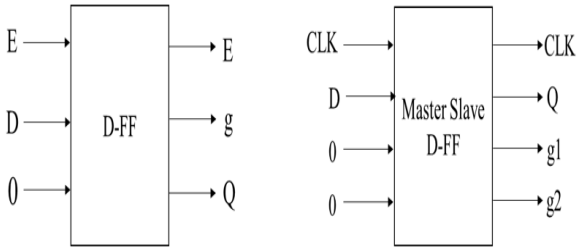

Fig. 9. Block diagram of D Flip-flop and master Slave D Flip-flop.

3.2. Serial input serial output (SISO) shift register

The SISO shift register is the simplest shift register output of a given flip-flop is connected to the data input of the next flip-flop on the application of clock at its right. The contents of the register are shifted by one-bit position to the right on application of clock pulse. The serial input is provided to the leftmost flip-flop i.e., first flip-flop and the serial output is the output of the rightmost one i.e., n-1 flip-flop. It accepts data in serial form and produces output serially. It takes n-1 clock pulses to store N-bit shift register and n-clock pulse to generate output. The reversible N-bit serial-in serial-out shift register for edge triggering and pulse triggering applications are depicted in Fig. 10 and Fig. 11, respectively. [10-11]

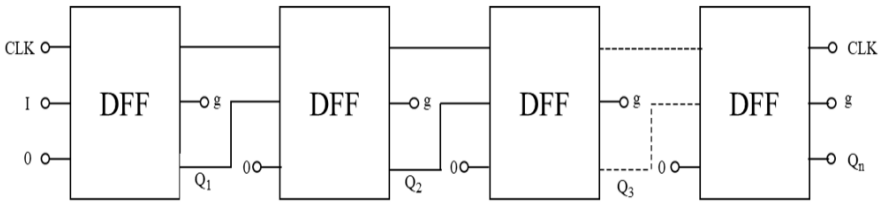

Fig. 10. Design of Edge-triggered N-bit SISO with D Flip-flop.

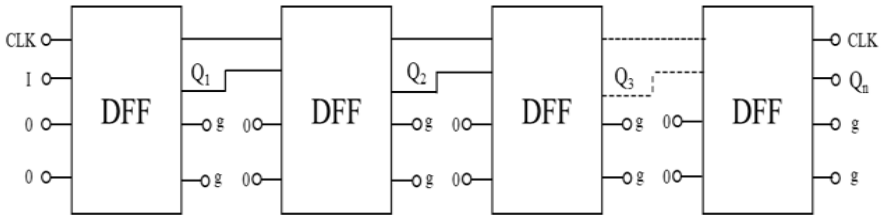

Fig. 11. Design of Pulse-triggered N-bit SISO with D Flip-flop.

3.3. Serial input parallel output (SIPO) shift register

A Serial-in Parallel-out shift register is like Serial-in Serial-out shift register. It is different in that it makes all the stored bits available as outputs. It will accept the information in serial mode, and it generates the output parallel. Data input appears on the register bit-by-bit basis whereas when data is stored in register hen all output appears in their respective flip-flop at a time. It takes n-1 clock pulse to store data in register and 1 clock pulse to reduce output. The Fig. 12 and 13 shows input is same as in SISO shift register and output appears as data, stored in shift register on a single clock pulse. [10-11]

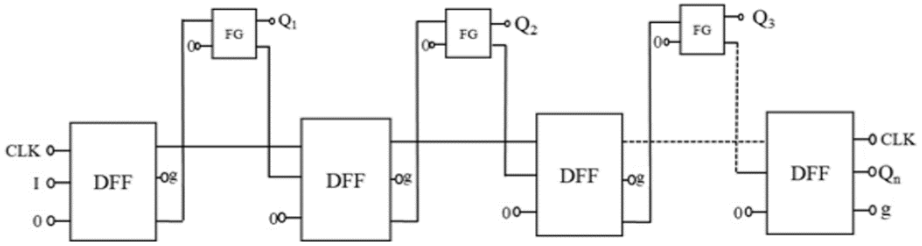

Fig. 12. Design of Edge Triggered N-bit SIPO with D-FF.

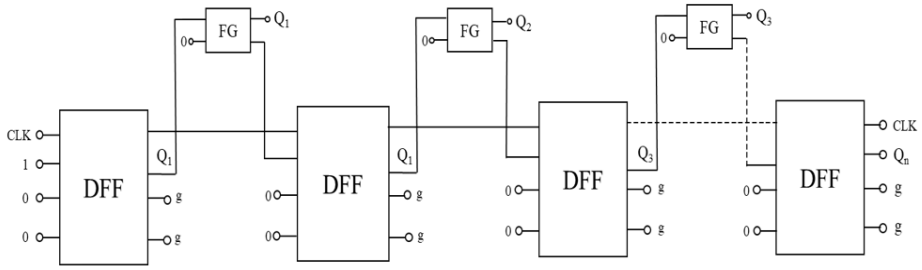

Fig. 13. Design of Edge Triggered N-bit SIPO with Master Slave D-FF.

4. Proposed reversible LFSR

Linear Feedback Shift Register (LFSR) is used to generate periodic sequence, but it does not produce all zero It can be constructed by doing exclusive-OR on the outputs of two or more flip-flops together and applying this output to one of the flip-flops. The design of 3-bit reversible LFSR is shown in Fig.14. Feynman gate is used between any two flip-flops to copy the output. It is also used to operate exclusive-OR operation on feedback path. Initially, Q1, Q2 and Q3 should not start with all zero, otherwise LFSR produces all 0-output pattern output for every clock pulse applied. The pattern count of LFSR equals to 2n-1, where n is the number of flip-flops. The patterns have an approximately equal number of 1's and 0's. Fig.15 and Table1 shows the simulation results of a 4-bit LFSR with Reversible Gates. The proposed 4-bit LFSR has the quantum cost of 50, garbage outputs 9 and delay of 50 ns. The elaborate design of a reversible 4-bit LFSR is depicted in Fig. 16.

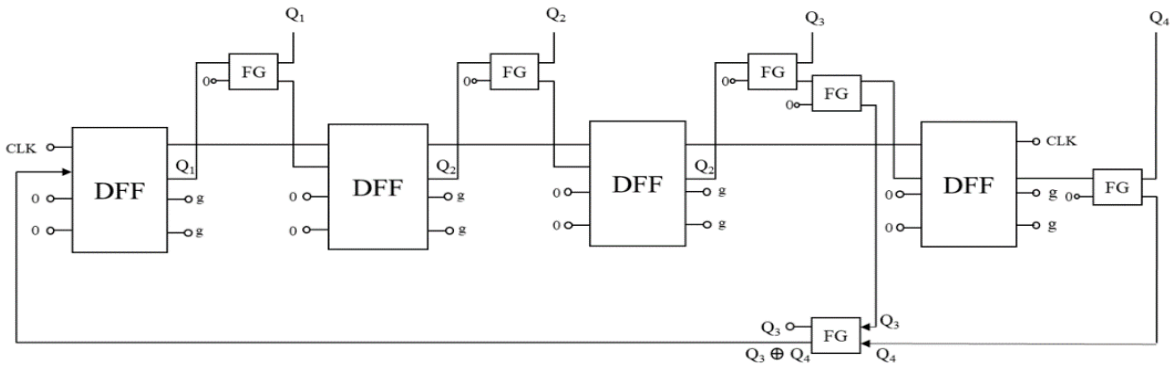

Fig. 14. Design of 4-bit LFSR with Reversible

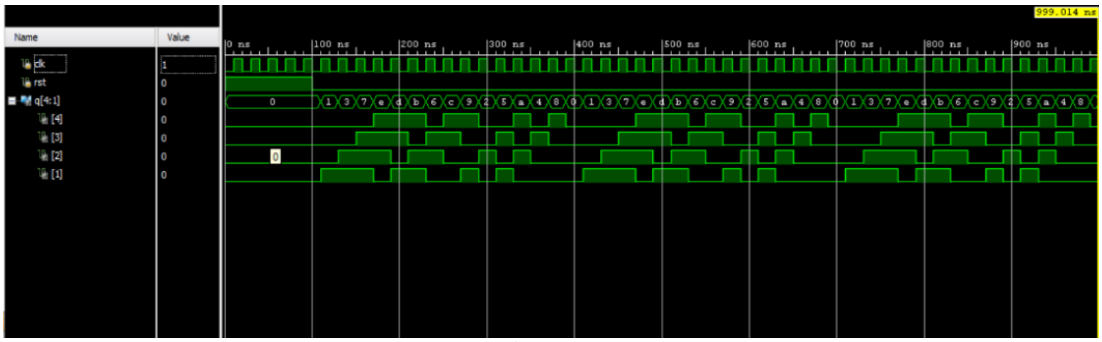

Fig. 15. Simulation results of a 4-bit LFSR with Reversible Gates

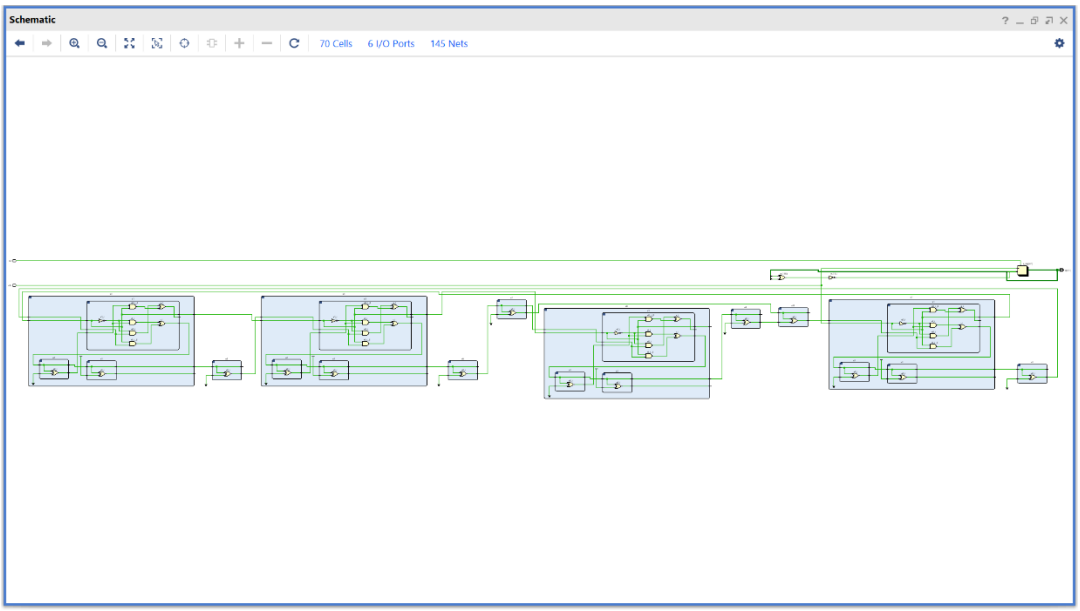

Fig. 16. Elaborate Design of a Reversible 4-bit LFSR.

5. CONCLUSION

The reversible circuits are the basic building blocks of quantum computers. This paper presents pulse triggered LFSR, which can produce a sequence of random bits which has a very long cycle because of its feedback path. To design higher complex computing circuits, this paper will be helpful for researches/designers. In this paper, we have demonstrated an optimized design of pulse and edge triggered SISO,SIPO registers and analyzed their quantum cost, garbage output and delay The paper can further be extended towards the digital design development using reversible logic circuits which are helpful in quantum computing, low power CMOS, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics. All these Simulation and synthesis processes are done successfully by using vivado 2016.4 and is tested on FPGA.

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